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HP Gareth REVA (HP SCH P/N:747866-000)

uATX(244 mm X 244 mm)

(MS-7932 11)

CPU: Intel Haswell Processor

System Chipset: Intel Lynx Point Chipset

OnBoard Chipset:
AZALIA Codec: Realtek ALC 221
LAN: Realtek RTL8151GH-CG 10/100/1000 NIC
SIO: Nuvoton NPCD379H
PCIe to PCI Bridge: ITE IT8893E
Flash ROM: 64 Mb

Main Memory: DDRIII (1333/1600MHz) * 2 (Dual Channel)

Expansion Slots:
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot *1

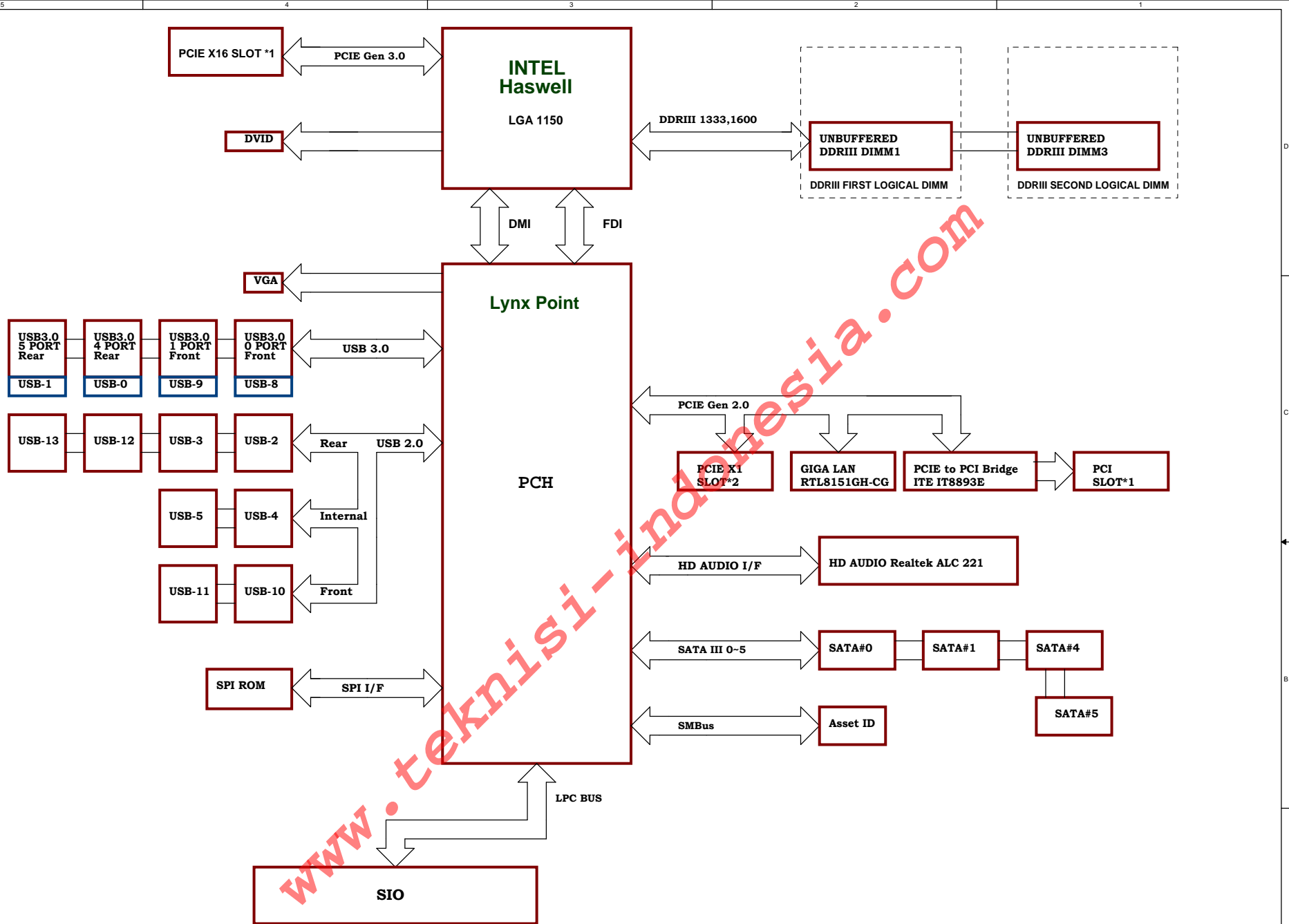
PWM:
Controller: ISL95816HRZ
Controller: NCP1587GDR2G

Other:
SATA *4
USB3.0 *4 (Rear*2 Front*2)
USB2.0 *8 (Rear*4 Front*2 Intrenal*2)
DVI PORT*1
VGA PORT *1
PRINT Header *1
COM PORT *1
COM Header *1

HP P/N	Description
747865-001	PCA,Gareth
747867-001	PCB,Gareth
747866-000	SCH,Gareth
747865-002	PCA,Gareth(G2)

BOM DISTRIBUTION RULE
GARETH
(BOM)

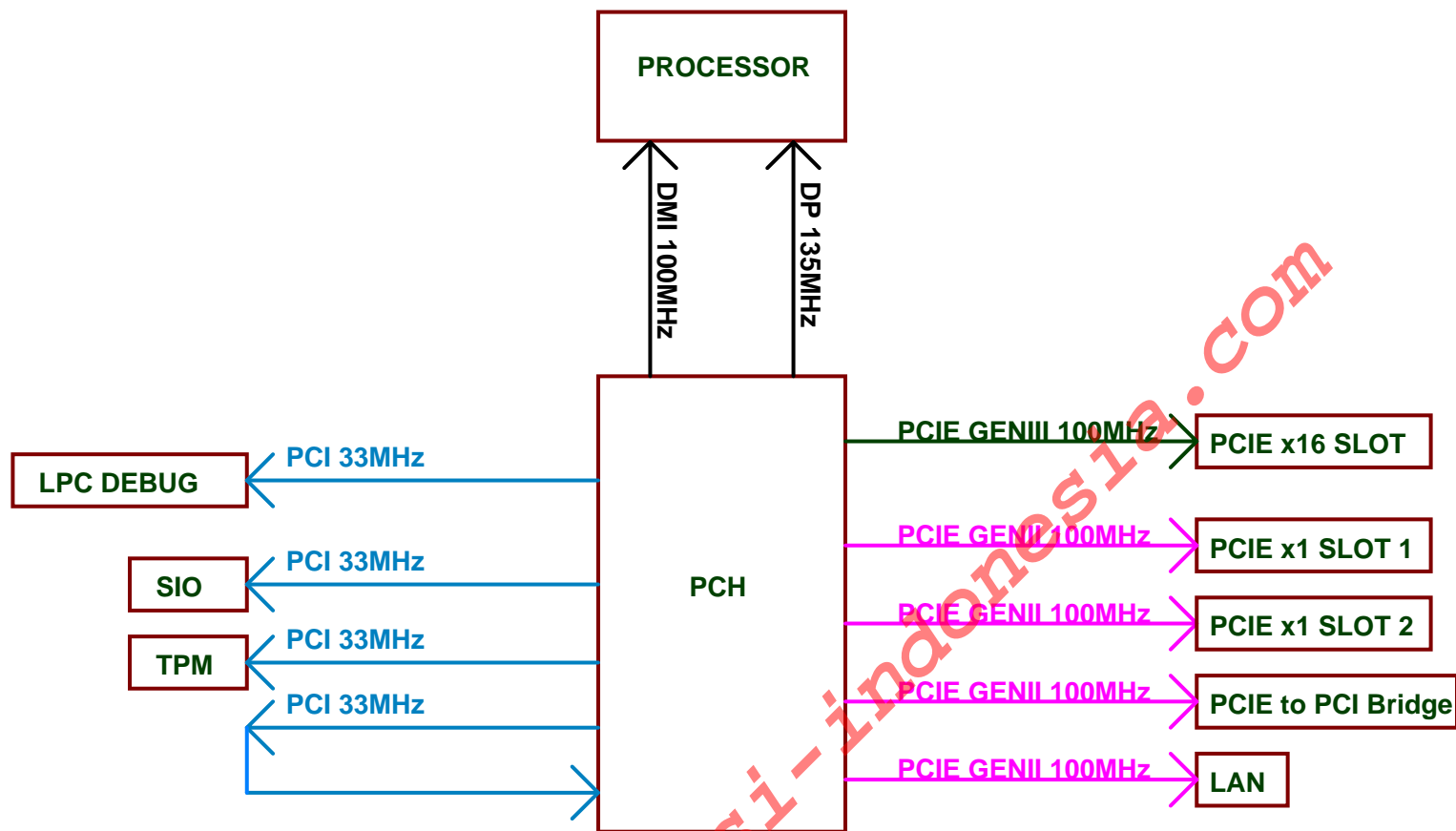
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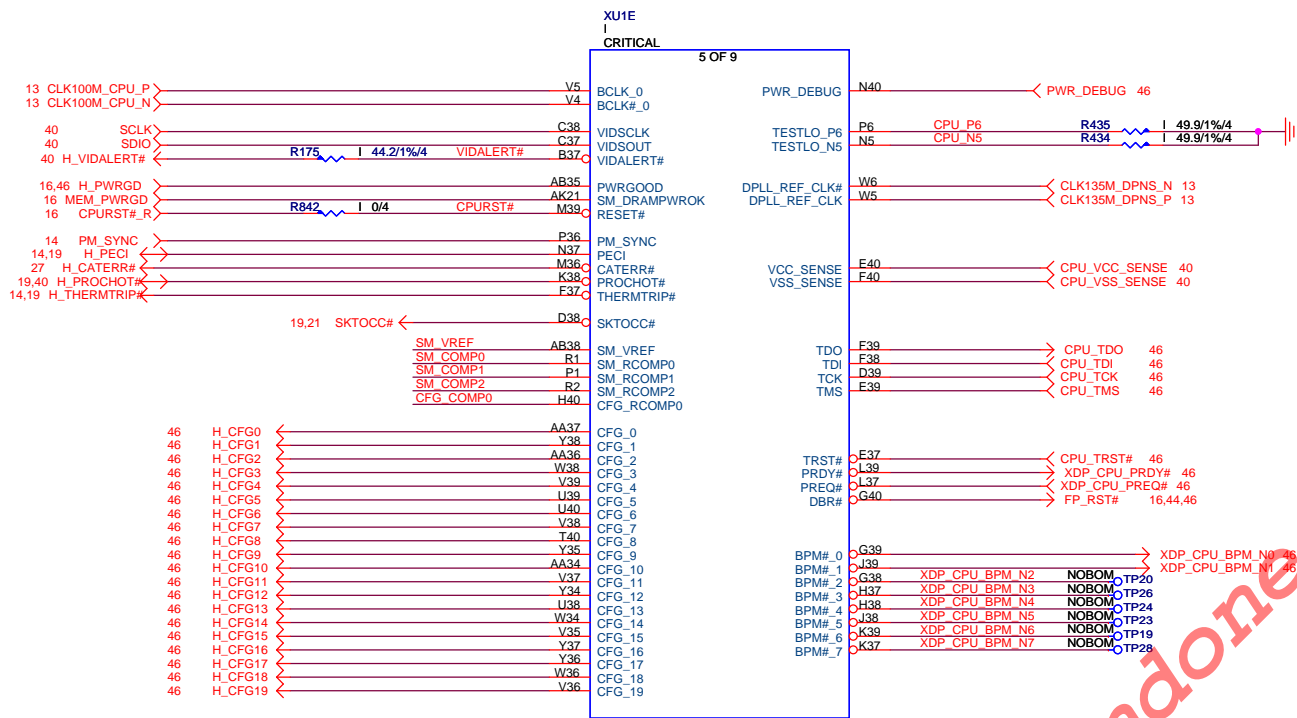
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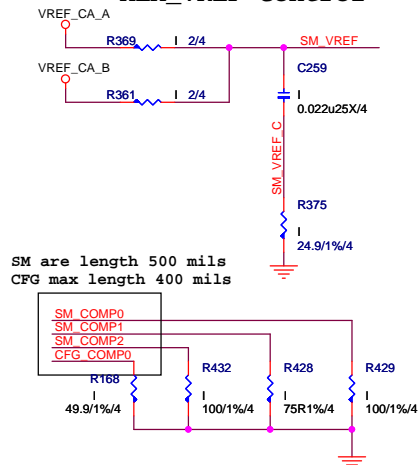
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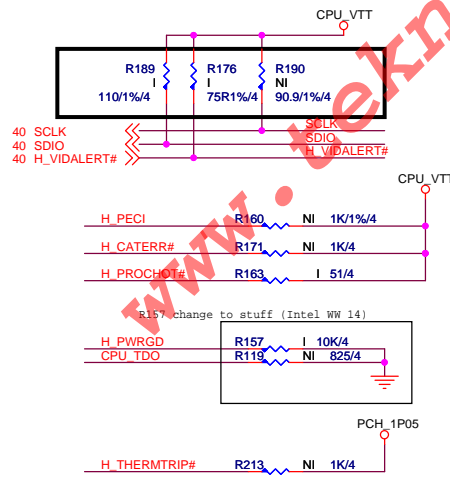


CPU2_2 N12-150A010-L06
AVL:N12-150A020-F02

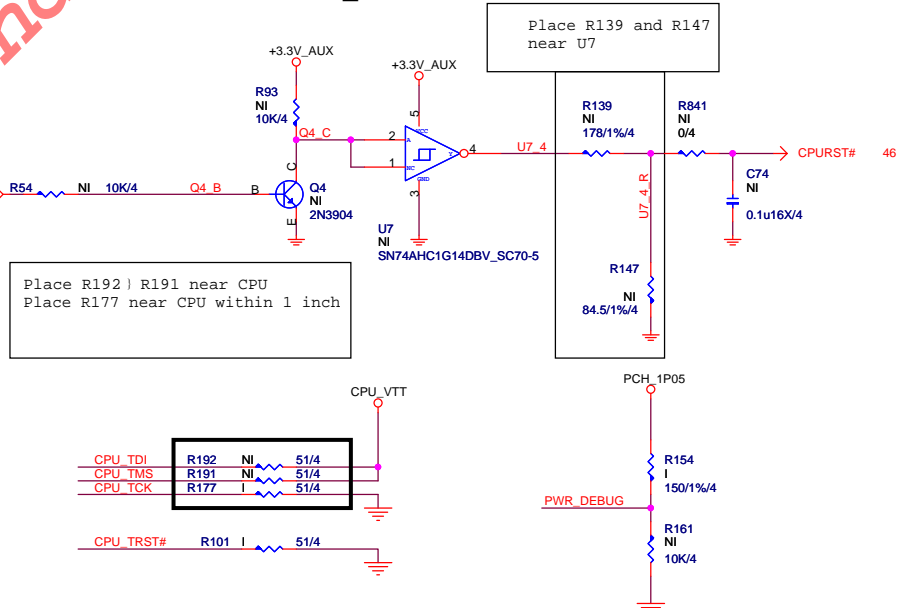
MEM_VREF Control



Place R189 | R176 | R190 near CPU



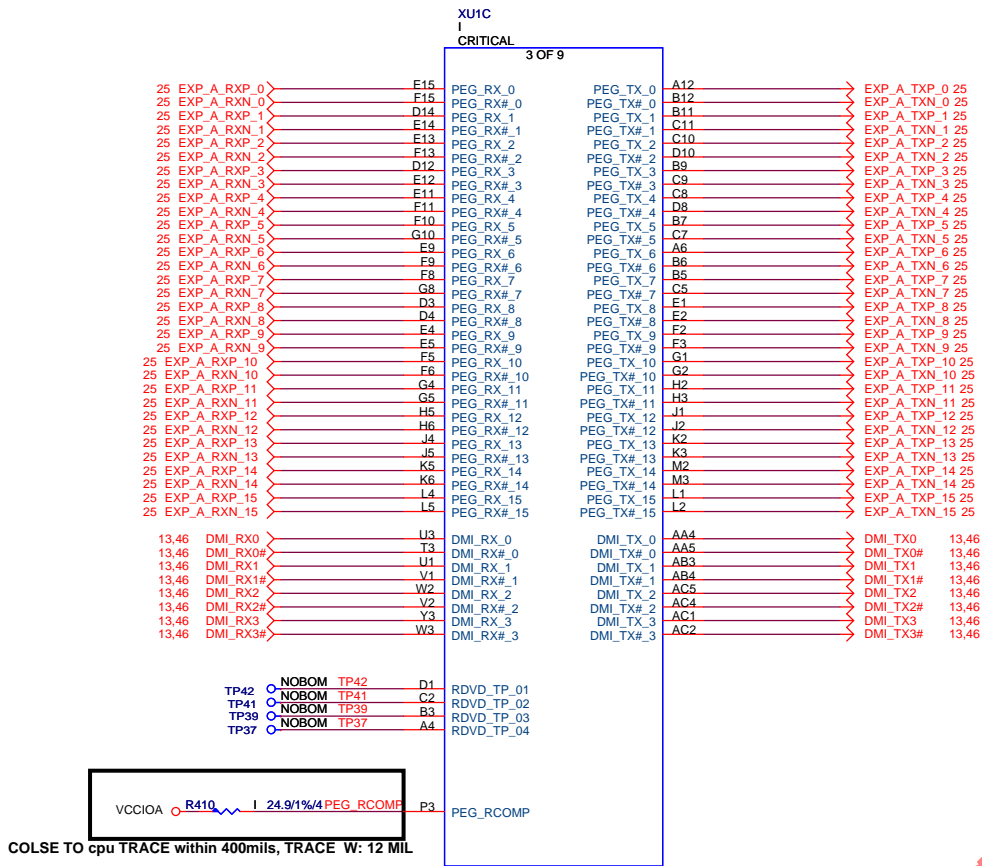
CPU_RESET#



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CPU-CLK/Control		
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N12-150A010-L06
AVL:N12-150A020-F02

COLSE TO cpu TRACE within 425mils, TRACE W: 12 MIL

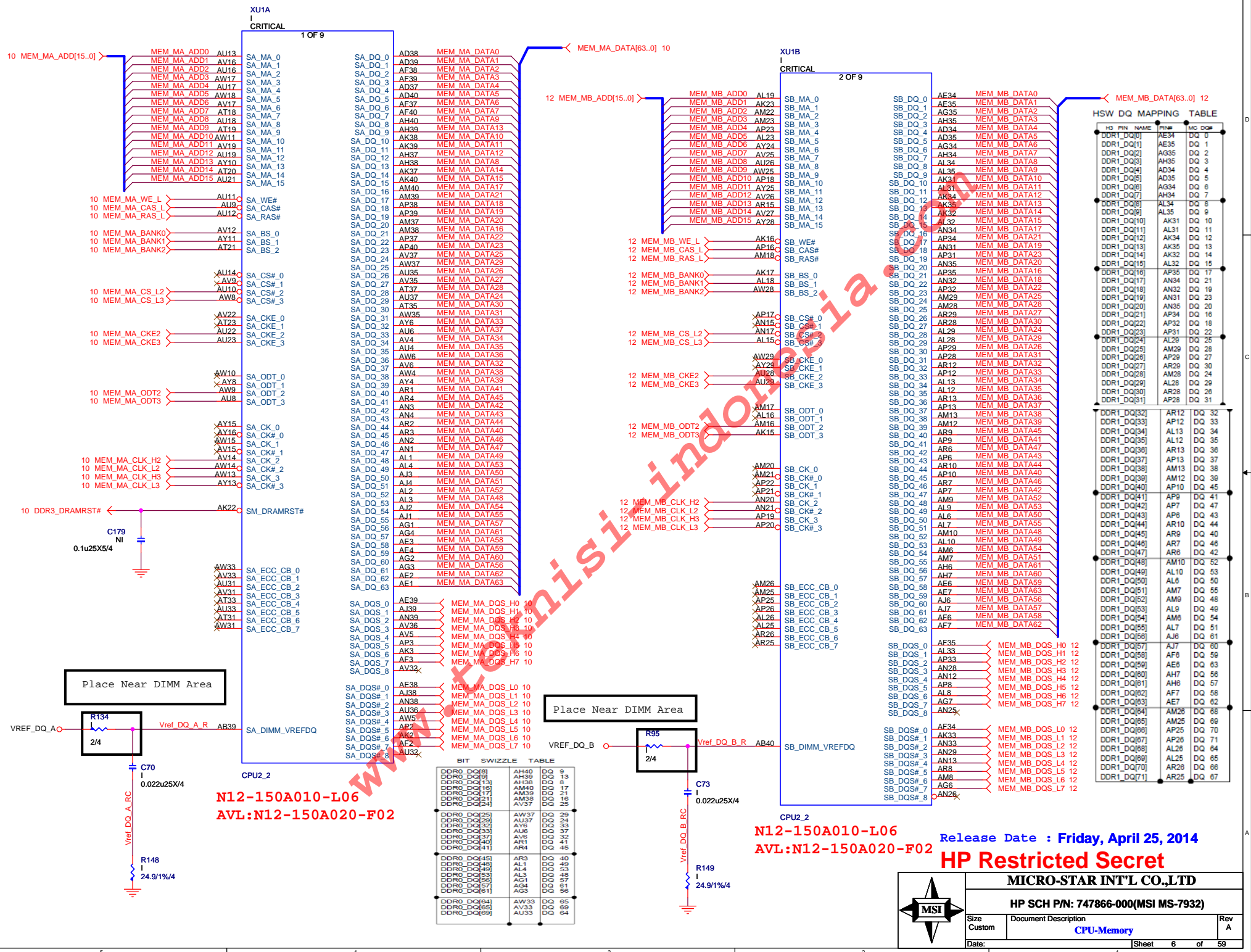
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AVL:N12-150A020-F02

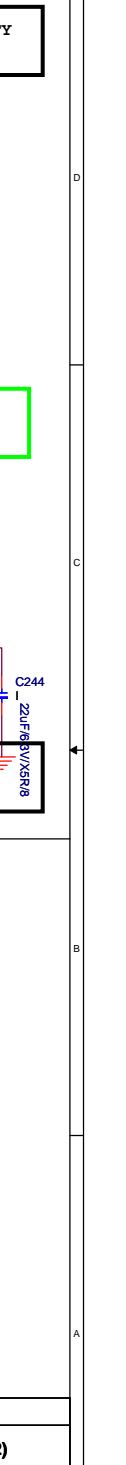
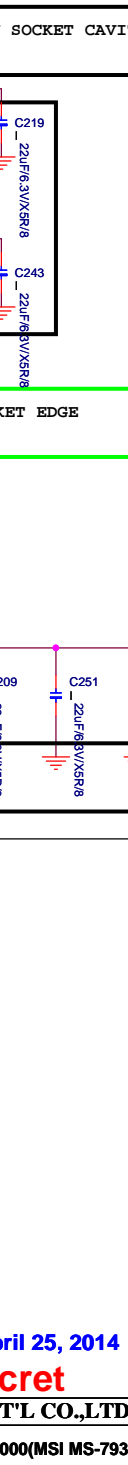
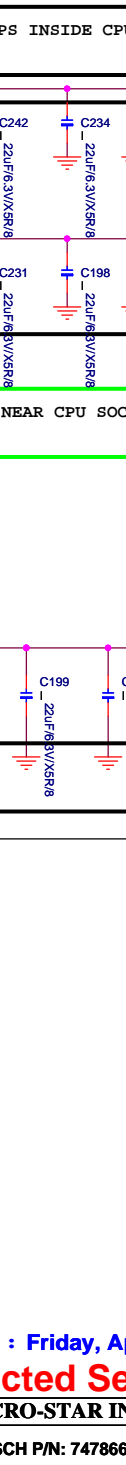
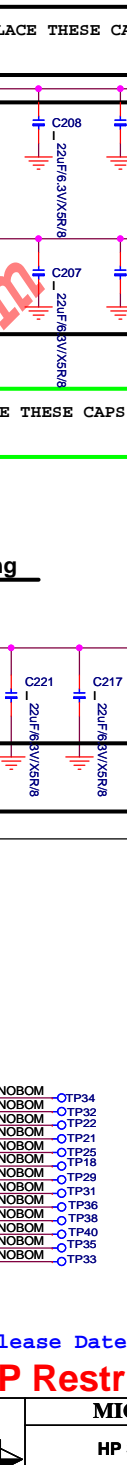
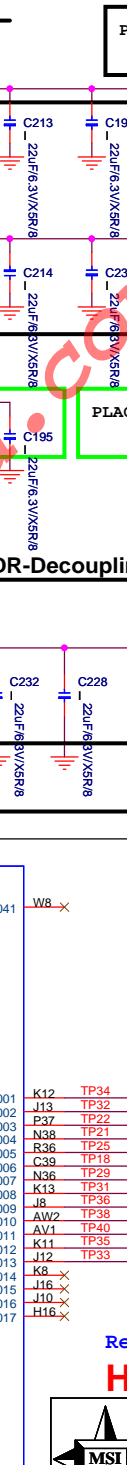
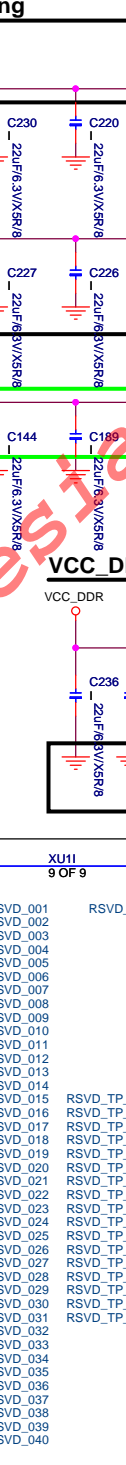
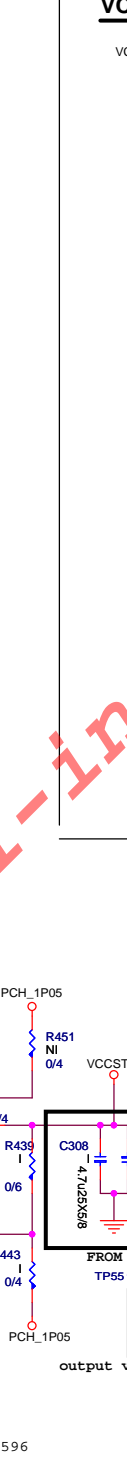
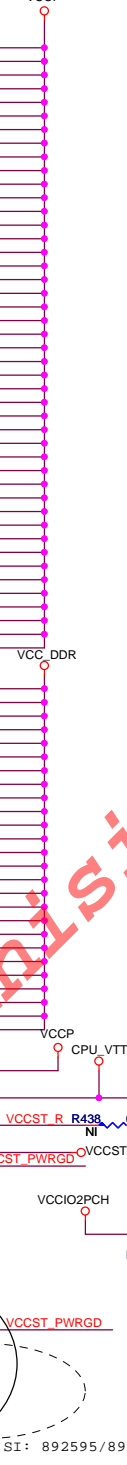
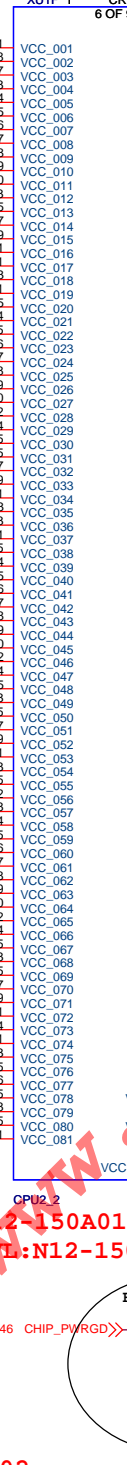
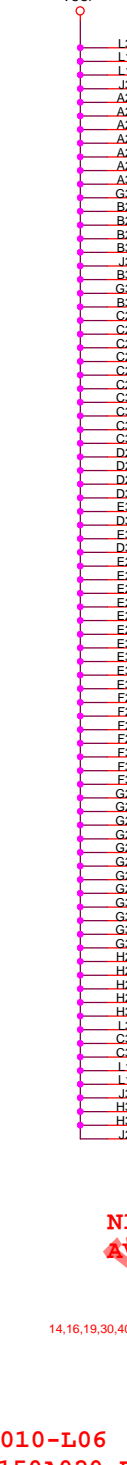
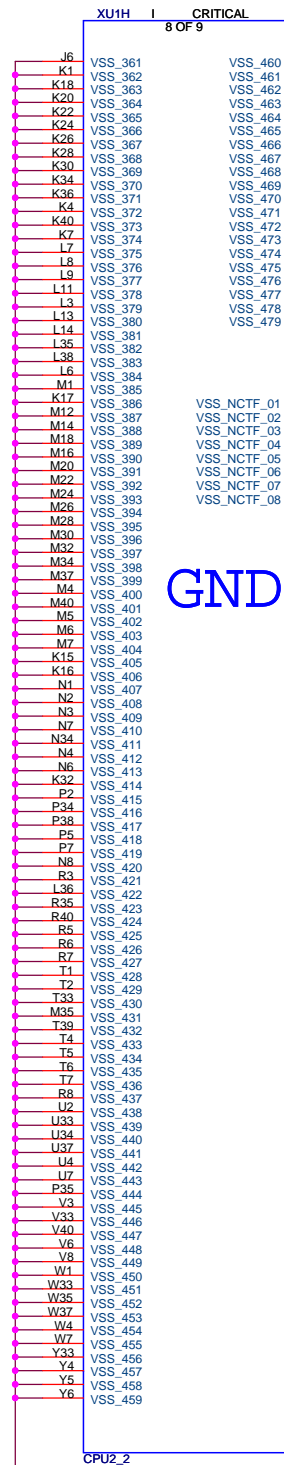
SI: 894794

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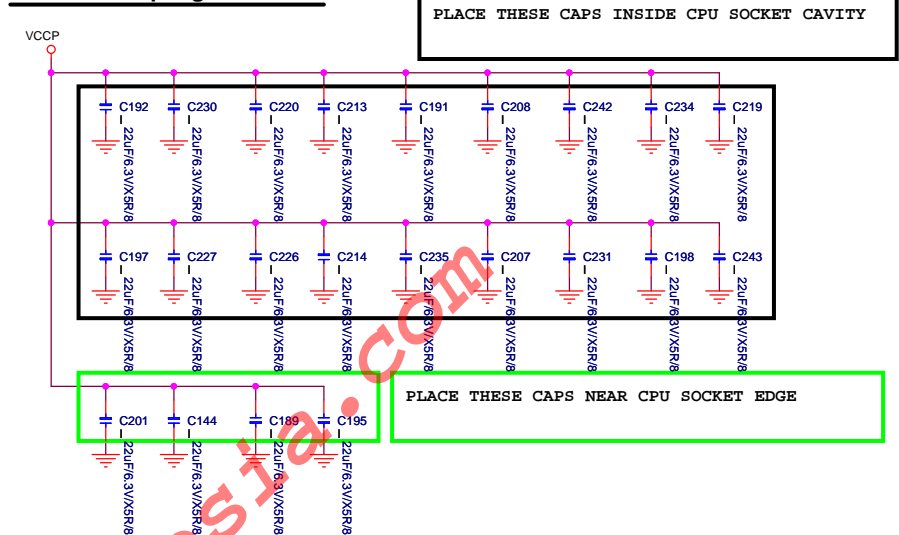
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Size Custom	Document Description			Rev A
CPU-PEG/MISC				
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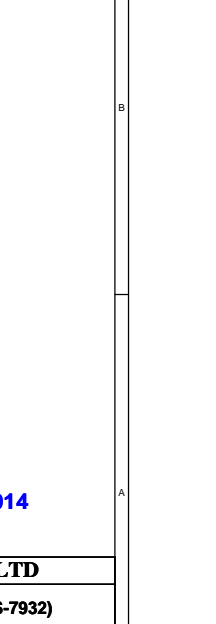
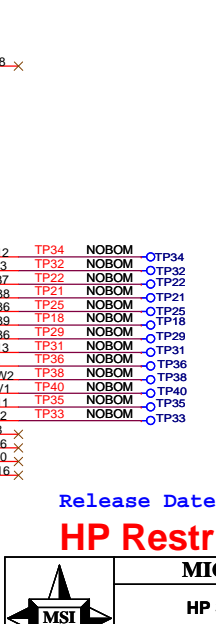
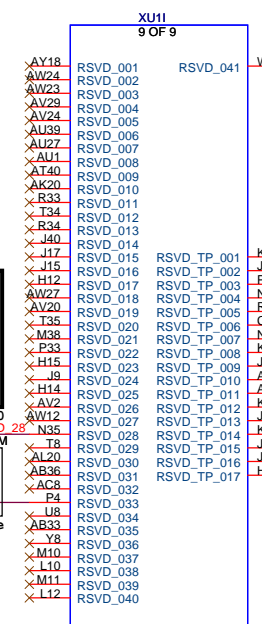
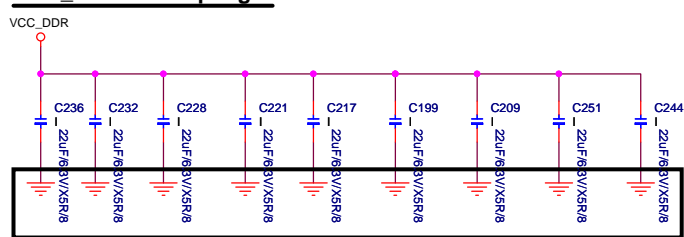




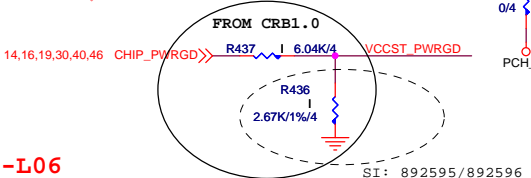
VCCP-Decoupling



VCC_DDR-Decoupling



N12-150A010-L06
AVL:N12-150A020-F02



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XU1G
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GND

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Size
Custom

Document Description
CPU-GND

Rev
A

Date:

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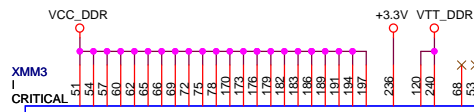
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Size Custom	Document Description Reserve	Rev A
Date:	Sheet 9 of 59	

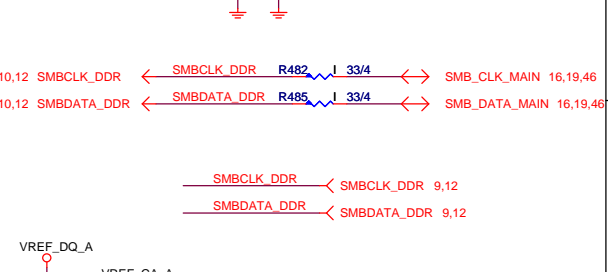
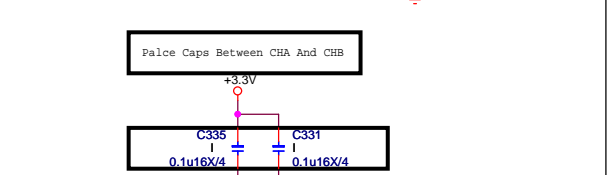
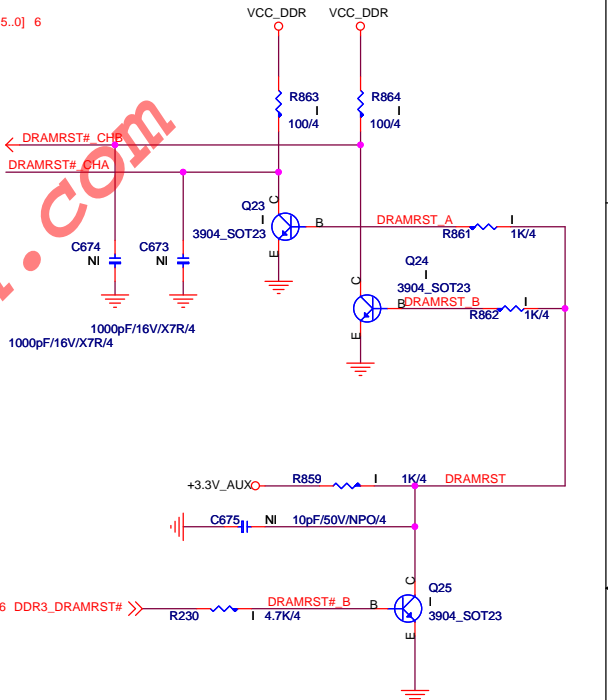
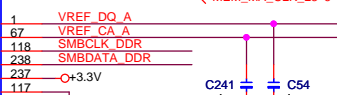
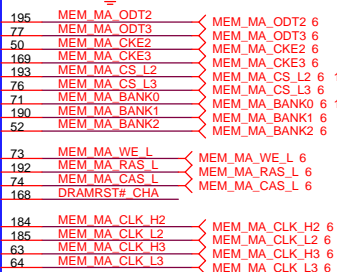
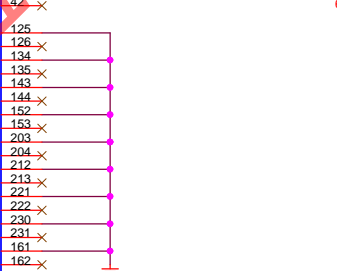
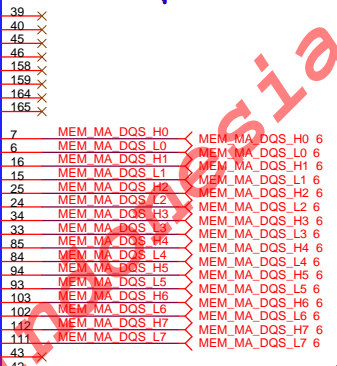
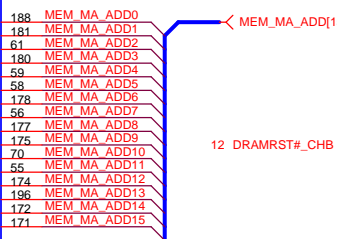
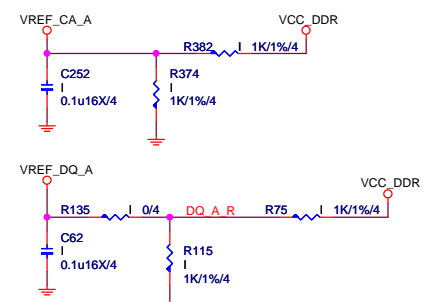
DDR3 DIMM_A2

6 MEM_MA_DATA[63..0] ← MEM_MA_DATA[63..0]



BLACK COLOR
N13-2401591-F02

DIMM SPD	
DIMM	Address [7:0]
XMM1	A0h
XMM3	A4h



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DDR3

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DDR III XMM3	
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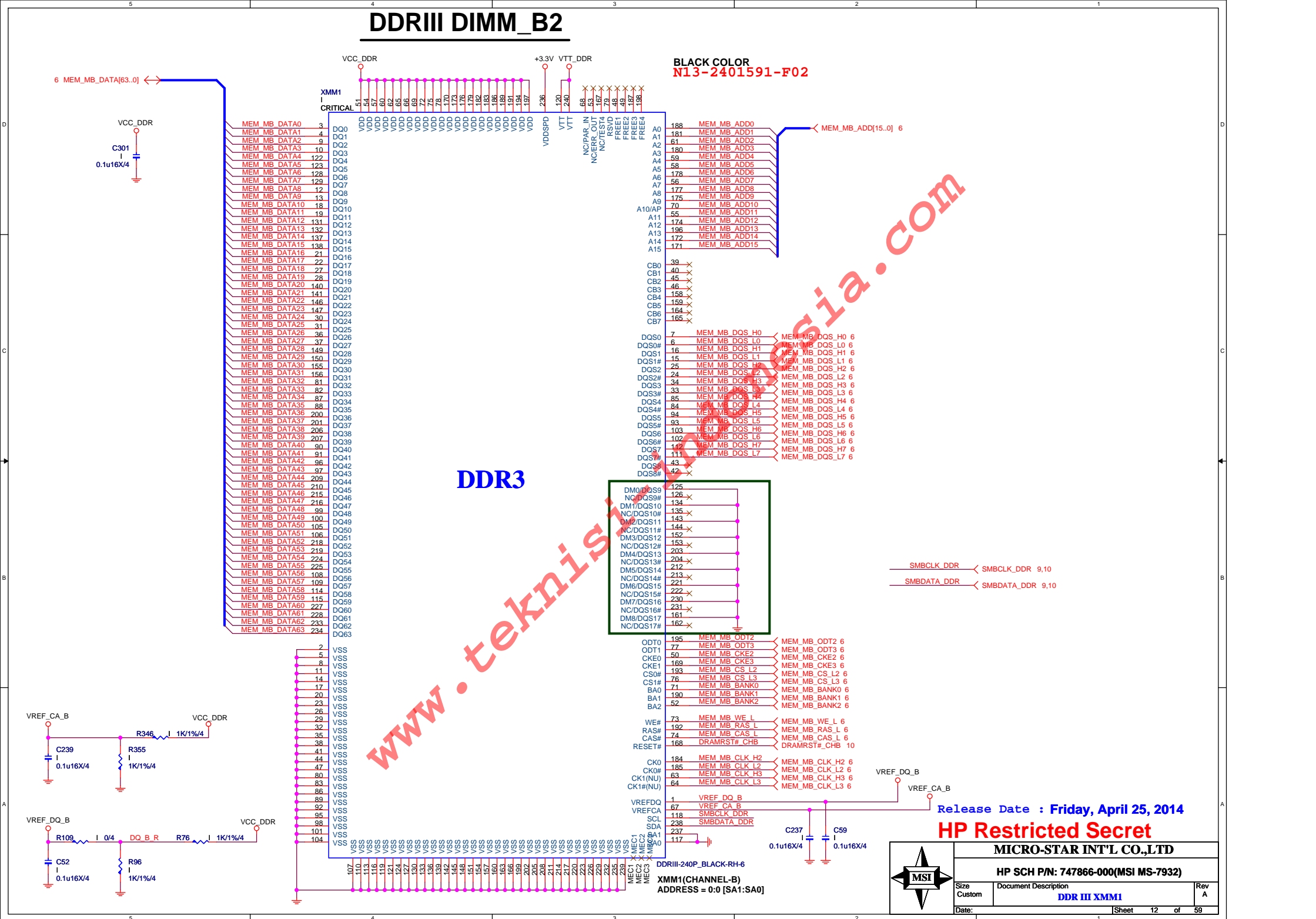
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Date:		Sheet 11 of 59	

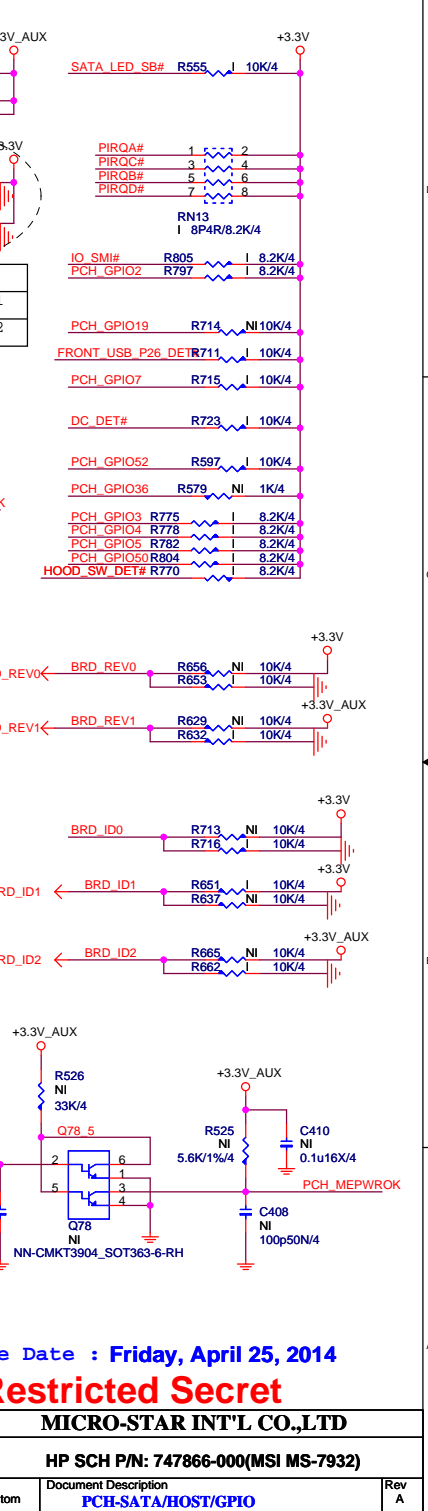
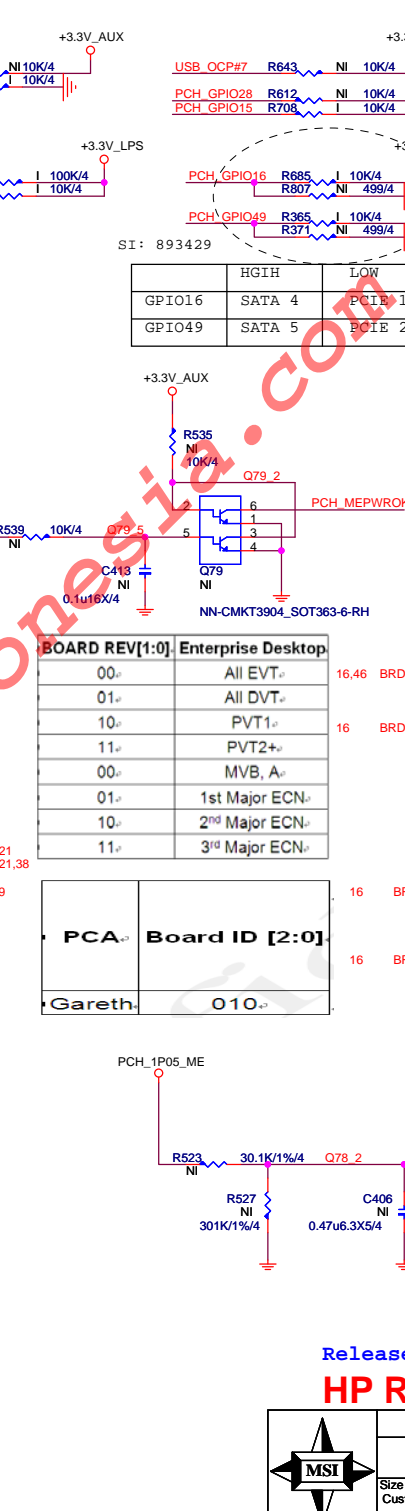
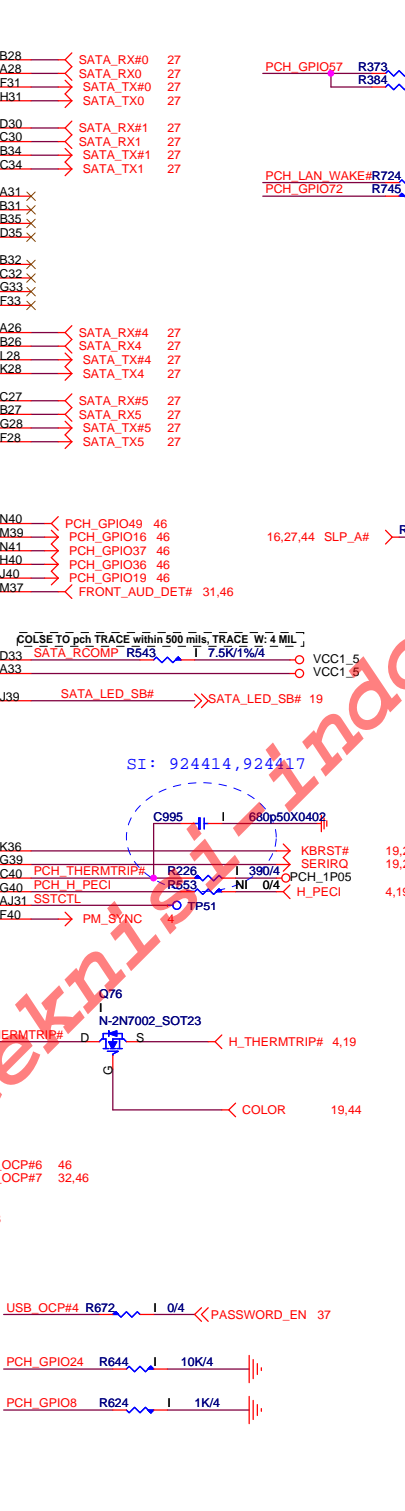
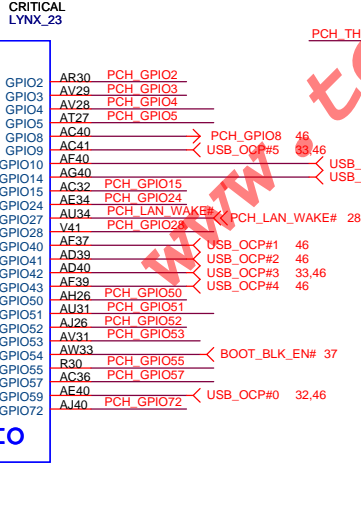
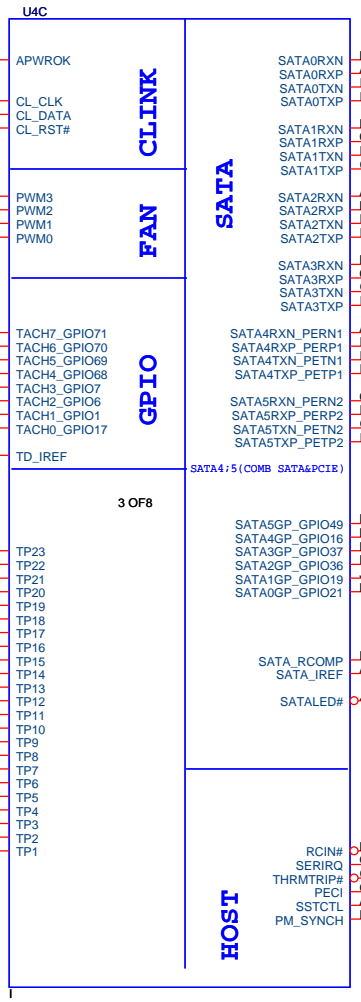
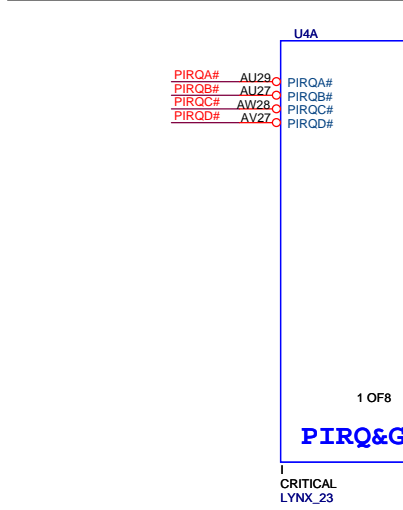
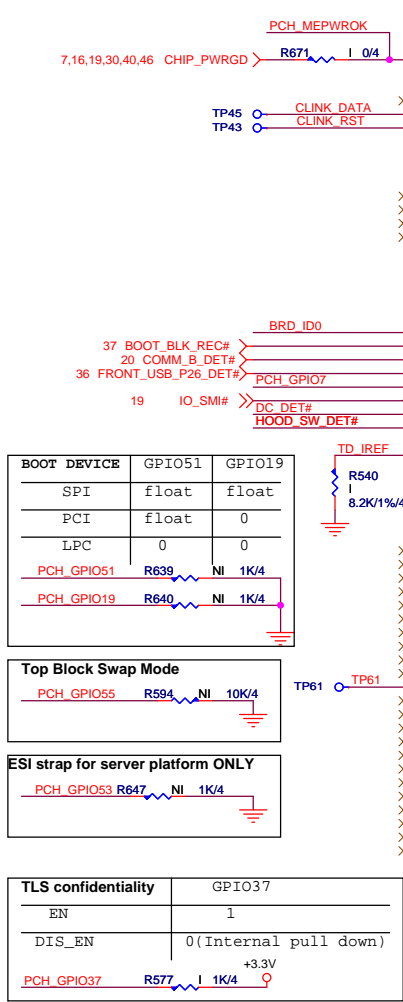
DDR3

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Size Custom	Document Description DDR III XMM1	Rev A
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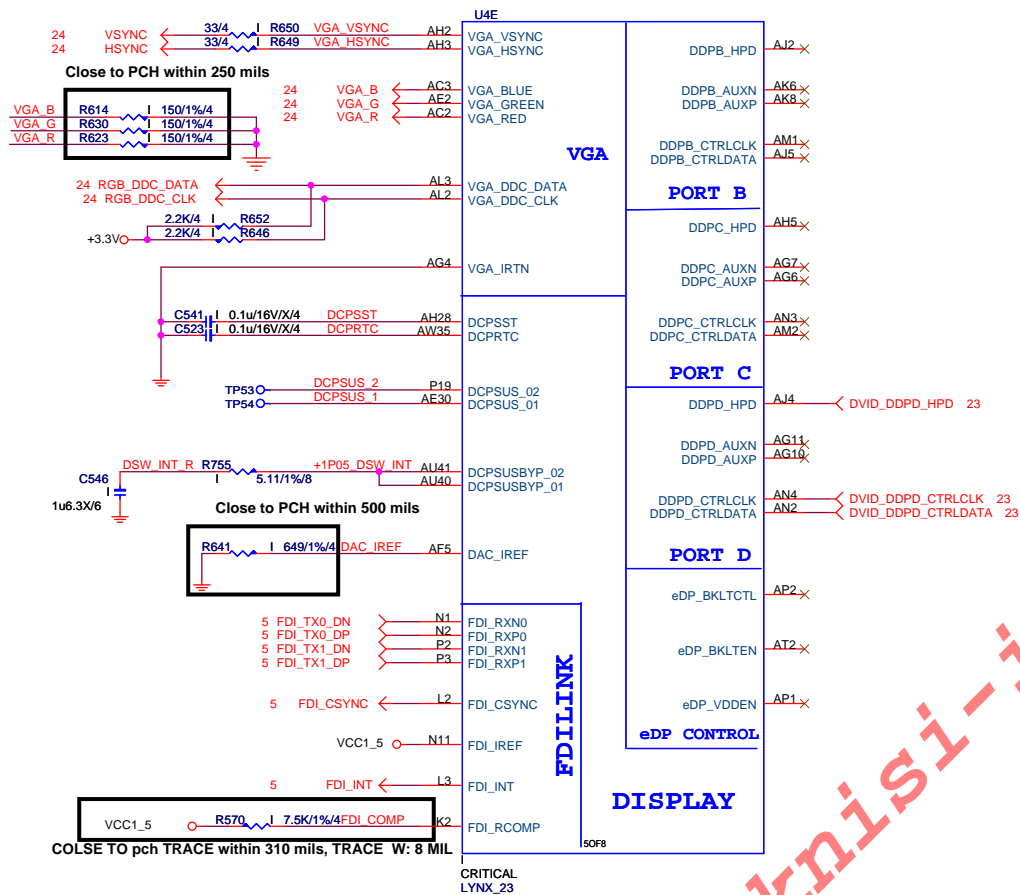
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PCH-SATA/HOST/GPIO

Size Custom Document Description Rev A

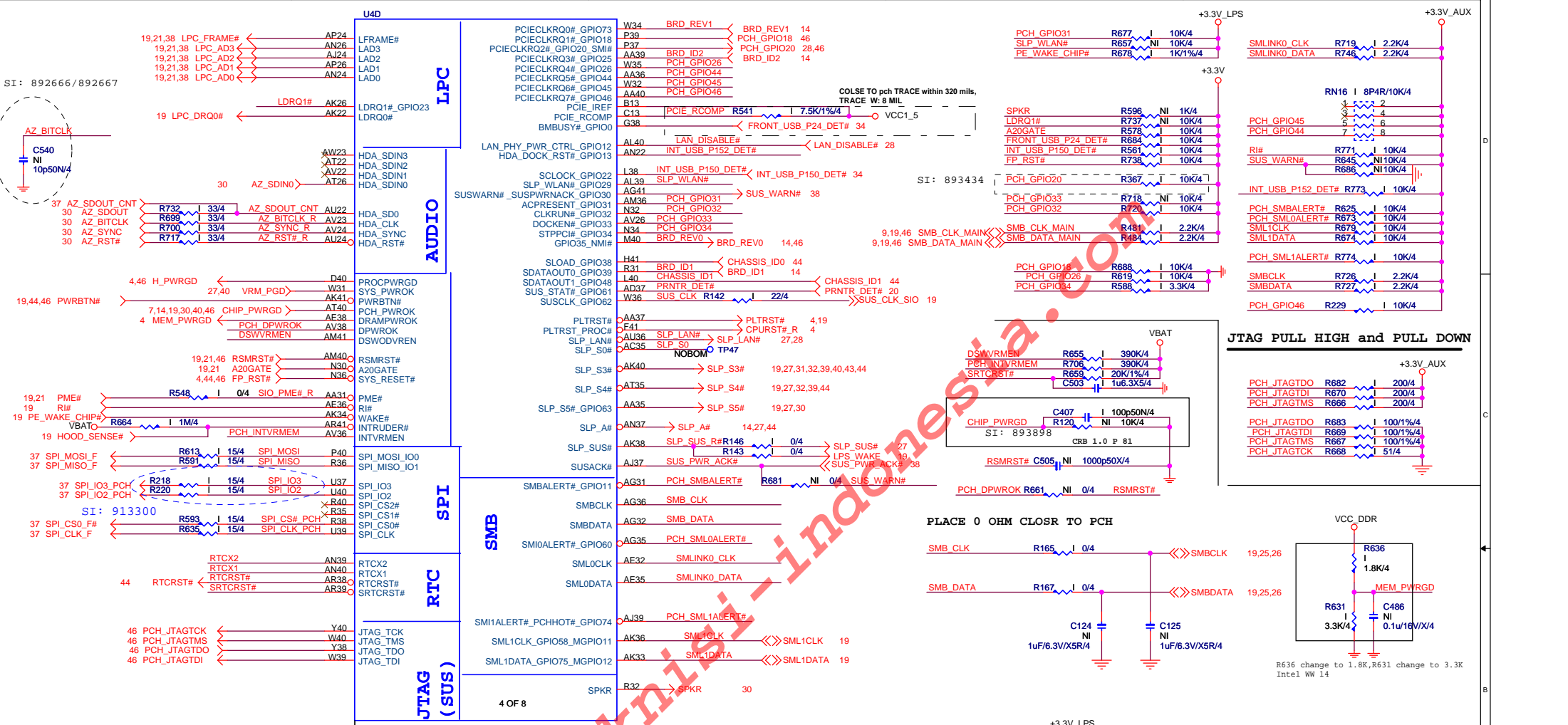
Date: Sheet 14 of 59



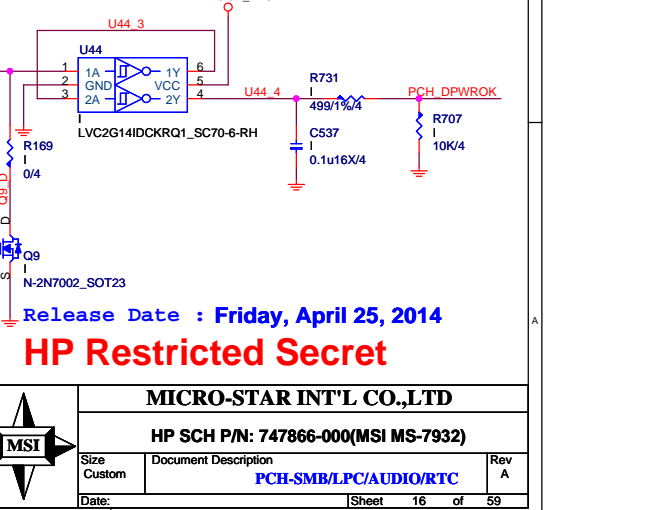
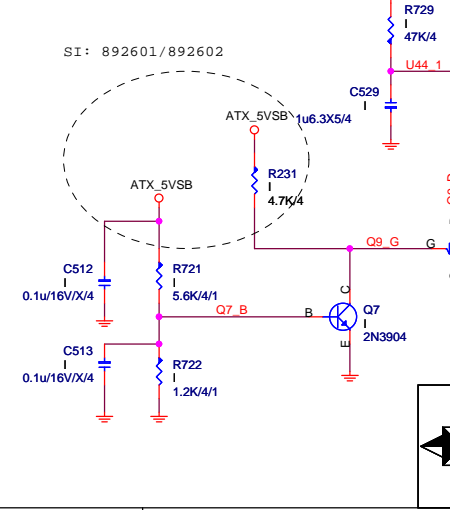
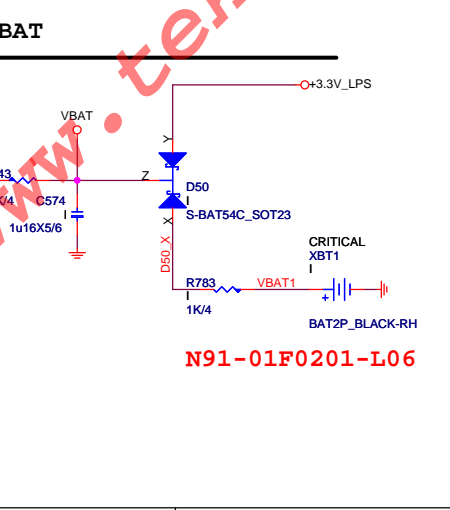
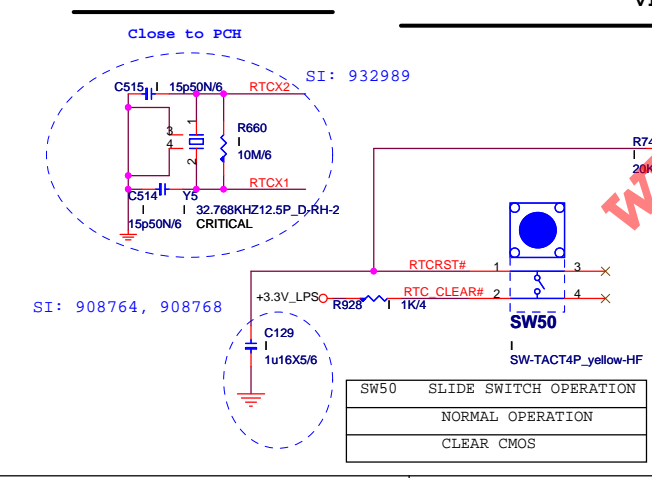
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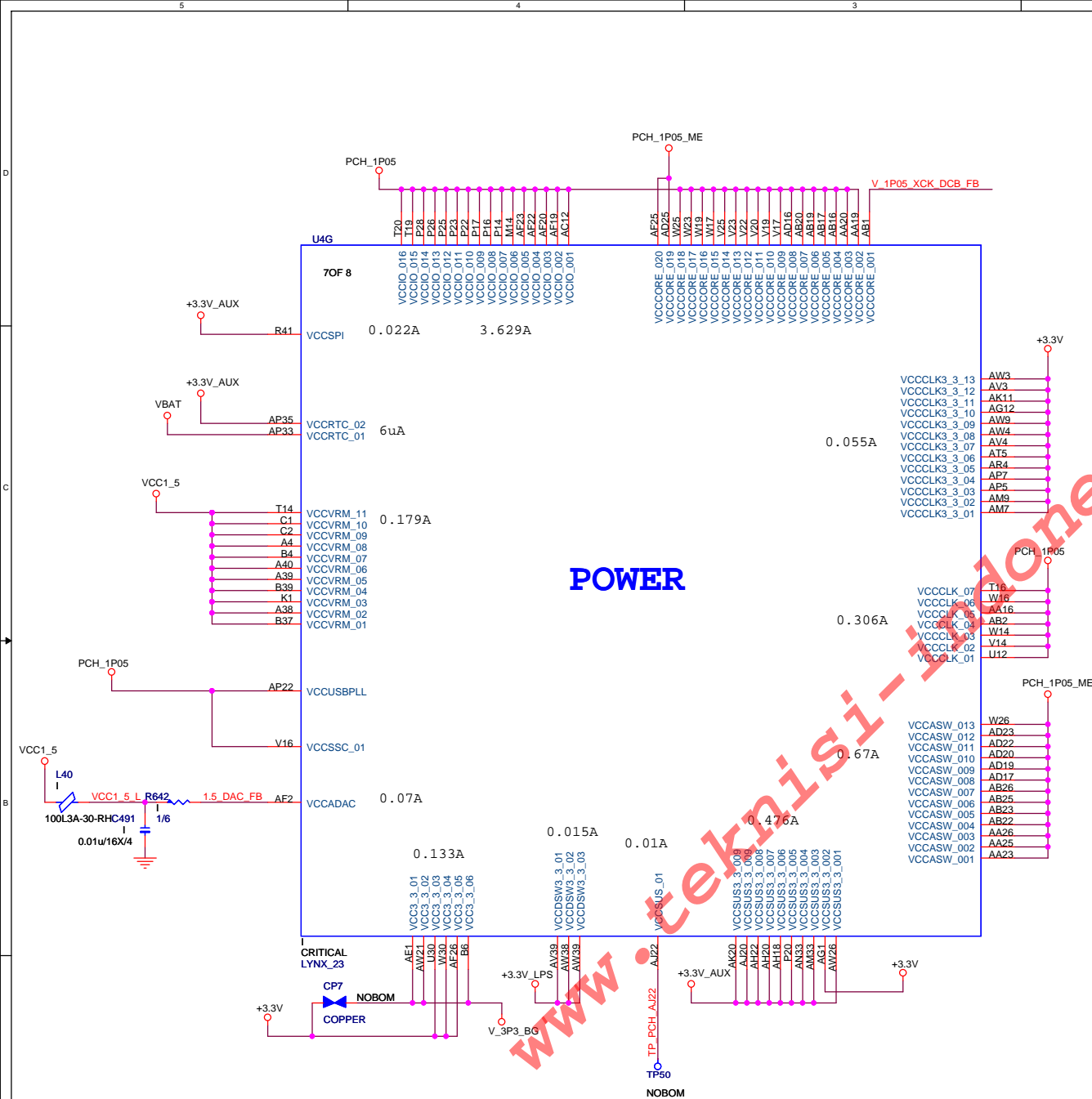
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RTC Block



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Place C283\ C237 near P14, P16, P17,P26, P28
C285 near M14 C288 near U12 C289 near W14
C291 near AB2 C295 near V16 C297 near AA16, W16
C300 near AP22, AF19

Place C303 near AV4, AR4, AT5, AP5
C634 near AG1 C633 near W30 C304 near AF26

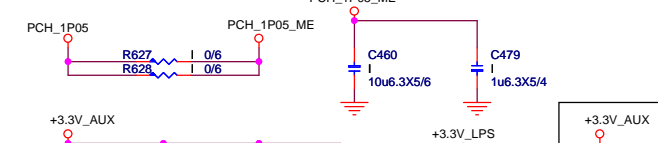
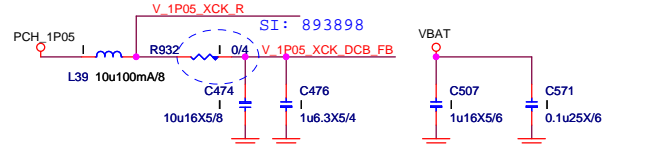
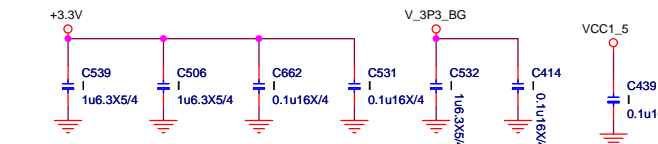
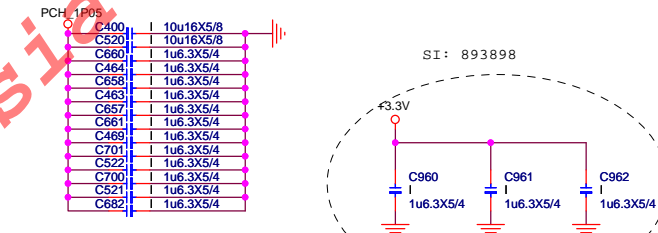
Place C630 near AN33 C301 near AK20
C631 near AW26 C302 near AP35

Place C635 near T14

Place C636 near AW39

Place C312\ C311 near AD17, AD19

Place C306 near AW21 C632 near B6



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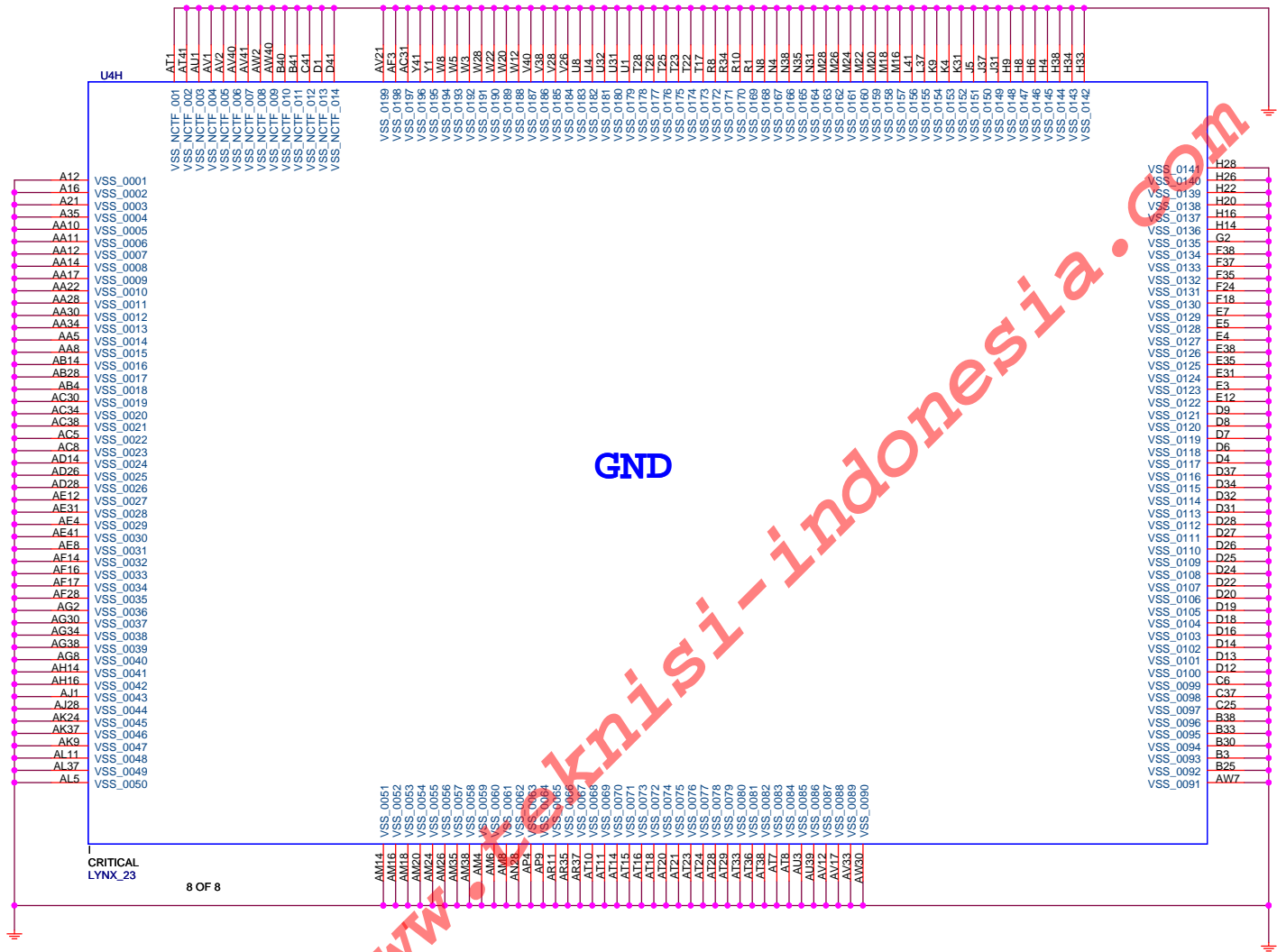
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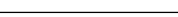


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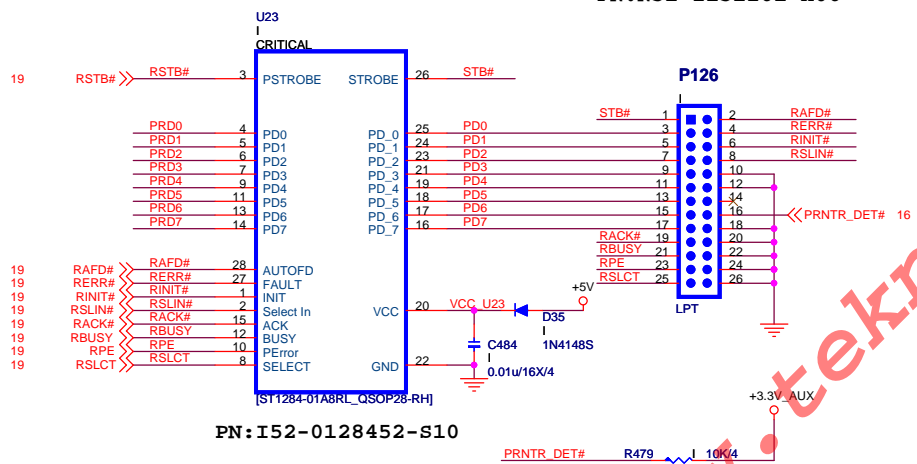
PN:B02-0379H04-NX9



SI: 892604/892605



PN:N31-2131261-H06



Parallel Port 2 x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

PD0	C721	NI 180p/50V/INPO/4
PD1	C668	NI 180p/50V/INPO/4
PD2	C718	NI 180p/50V/INPO/4
PD3	C719	NI 180p/50V/INPO/4
PD4	C720	NI 180p/50V/INPO/4
PD5	C722	NI 180p/50V/INPO/4
PD6	C664	NI 180p/50V/INPO/4
PD7	C717	NI 180p/50V/INPO/4
STB#	C716	NI 180p/50V/INPO/4
RACK#	C704	NI 180p/50V/INPO/4
RBUSY	C712	NI 180p/50V/INPO/4
RPE	C713	NI 180p/50V/INPO/4
RACFT	C714	NI 180p/50V/INPO/4
RACFD	C715	NI 180p/50V/INPO/4
RERR#	C681	NI 180p/50V/INPO/4
RSLSN#	C708	NI 180p/50V/INPO/4

U31
CRITICAL

PN: I95-7518562-U07

75185L-TSSOP20_T

PN: N51-09M0211-F02

SERIAL PORT 2

10 P52

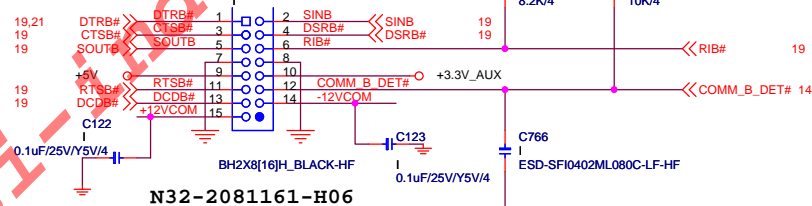
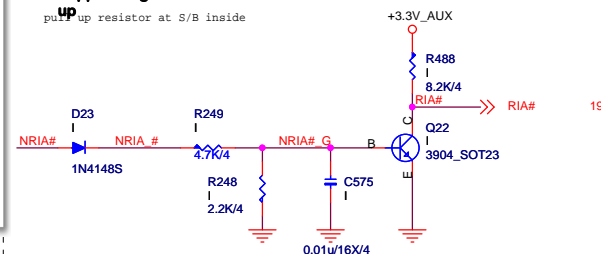


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCB#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

Support ring wake up
pull up resistor at S/



Release Date : Friday, April 25, 2014

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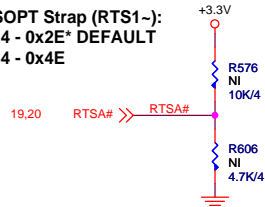
MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 747866-000(MSI MS-7932)

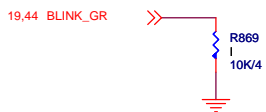
Size Custom	Document Description KB / MS / COM / LPT
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Date:	Sheet 20 of 59
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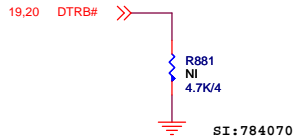
SYSOPT Strap (RTS1~):
R124 - 0x2E* DEFAULT
R144 - 0x4E



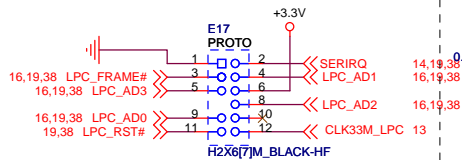
- 10 K Ω ¹ external pull-up resistor - Workstations pins default.
- 10 K Ω ¹ external pull-down resistor - Desktop pins default.



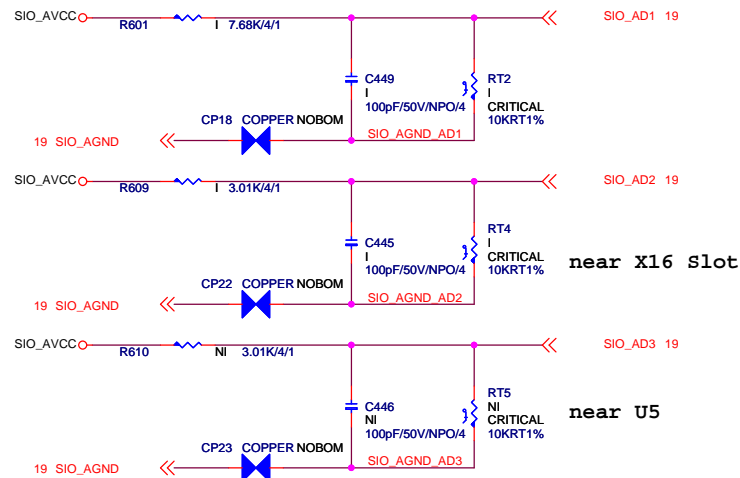
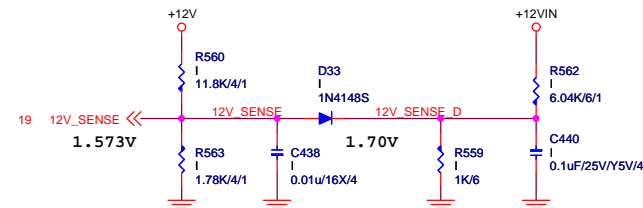
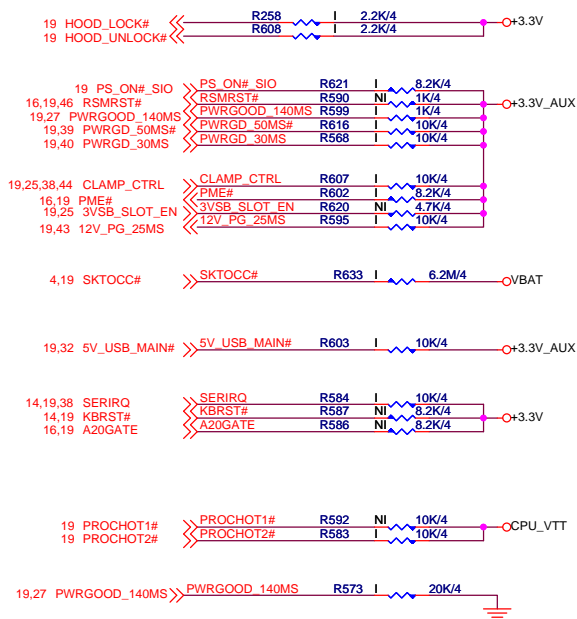
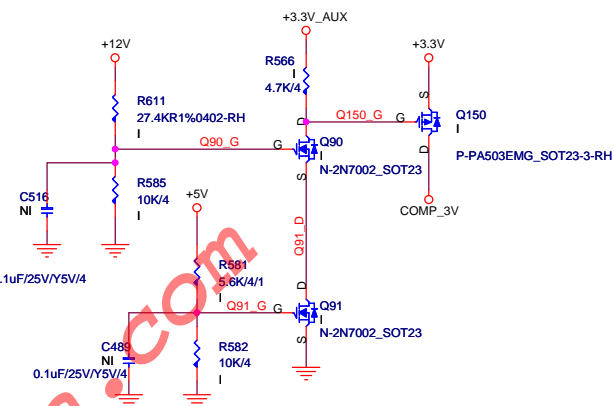
- No pull-down resistor (default) - normal device operation.
- 4.7 K Ω external pull-down resistor- JTAG selected.



LPC Debug



N31-2061311-H06



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Size Custom	Document Description SIO- PULL UP/DOWN/PS_ON	Rev A
Date:	Sheet 21 of 59	

19 PS_ON#_SIO >> PS_ON#_SIO R574 0/4 >> PS_ON# 27,44

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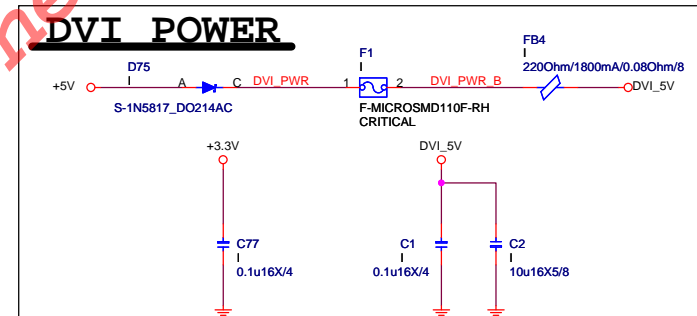
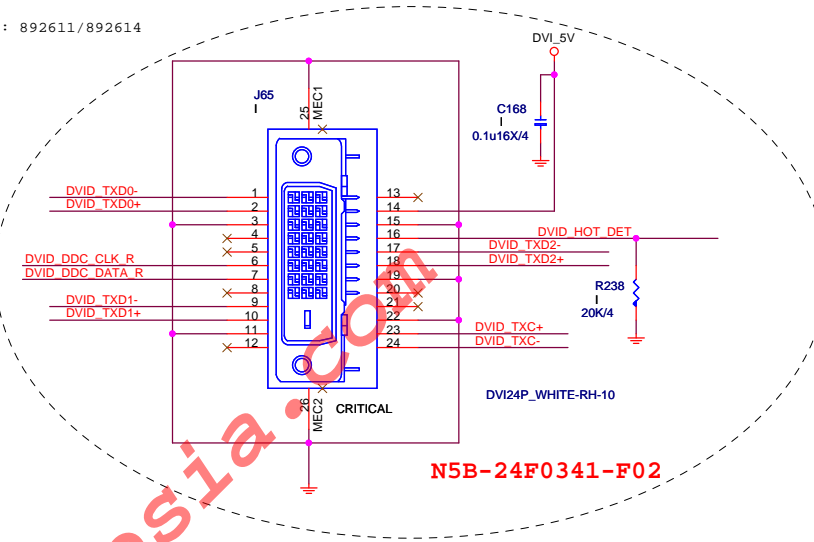
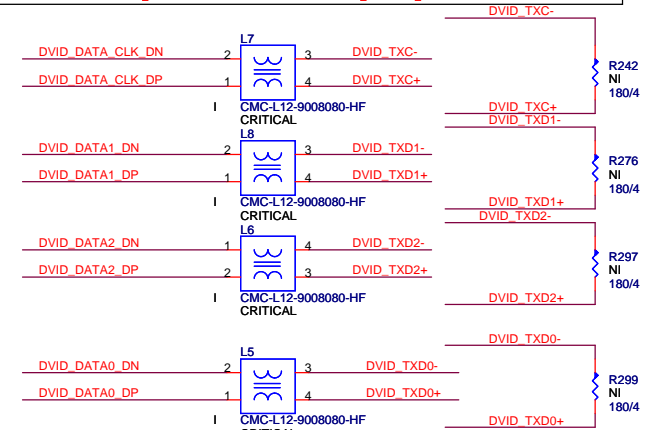
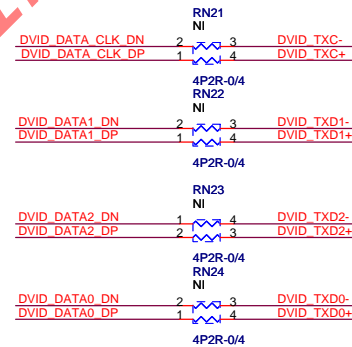
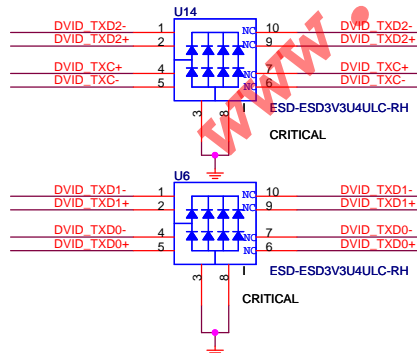
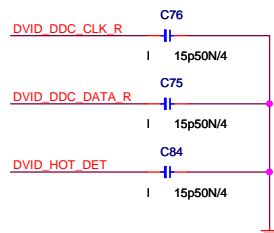
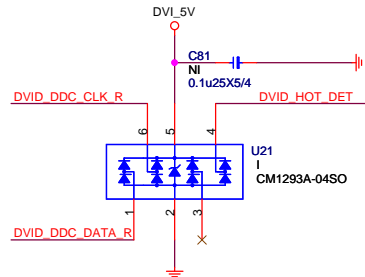
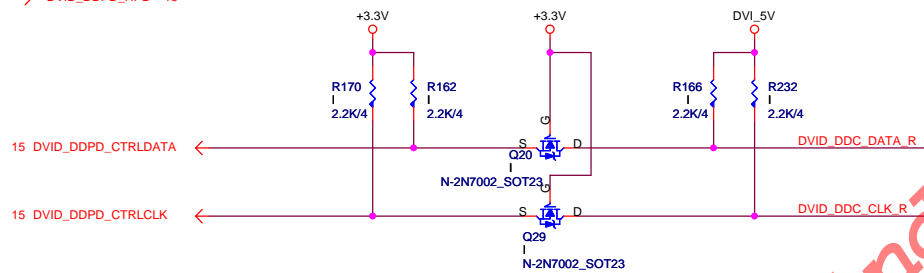
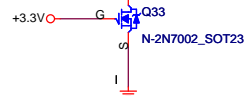
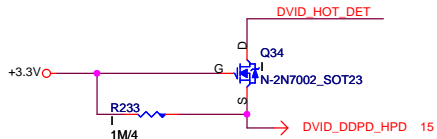
	MICRO-STAR INT'L CO.,LTD		
	HP SCH P/N: 747866-000(MSI MS-7932)		
	Size Custom	Document Description DDI Port Slot	Rev A
Date:		Sheet 22 of 59	

DVID level shifter

SI: 892611/892614

5 DVID_DDPD_CLK_P C66 0.1u16X/4 DVID_DATA_CLK_DP
 5 DVID_DDPD_CLK_N C69 0.1u16X/4 DVID_DATA_CLK_DN
 5 DVID_DDPD_TX2_P C56 0.1u16X/4 DVID_DATA2_DP
 5 DVID_DDPD_TX2_N C57 0.1u16X/4 DVID_DATA2_DN
 5 DVID_DDPD_TX1_P C58 0.1u16X/4 DVID_DATA1_DP
 5 DVID_DDPD_TX1_N C61 0.1u16X/4 DVID_DATA1_DN
 5 DVID_DDPD_TX0_P C51 0.1u16X/4 DVID_DATA0_DP
 5 DVID_DDPD_TX0_N C53 0.1u16X/4 DVID_DATA0_DN

Q33_D R181 680/4 DVID_DATA_CLK_DN
 R164 680/4 DVID_DATA_CLK_DP
 R173 680/4 DVID_DATA1_DN
 R138 680/4 DVID_DATA1_DP
 R140 680/4 DVID_DATA2_DN
 R172 680/4 DVID_DATA2_DP
 R103 680/4 DVID_DATA0_DN
 R112 680/4 DVID_DATA0_DP

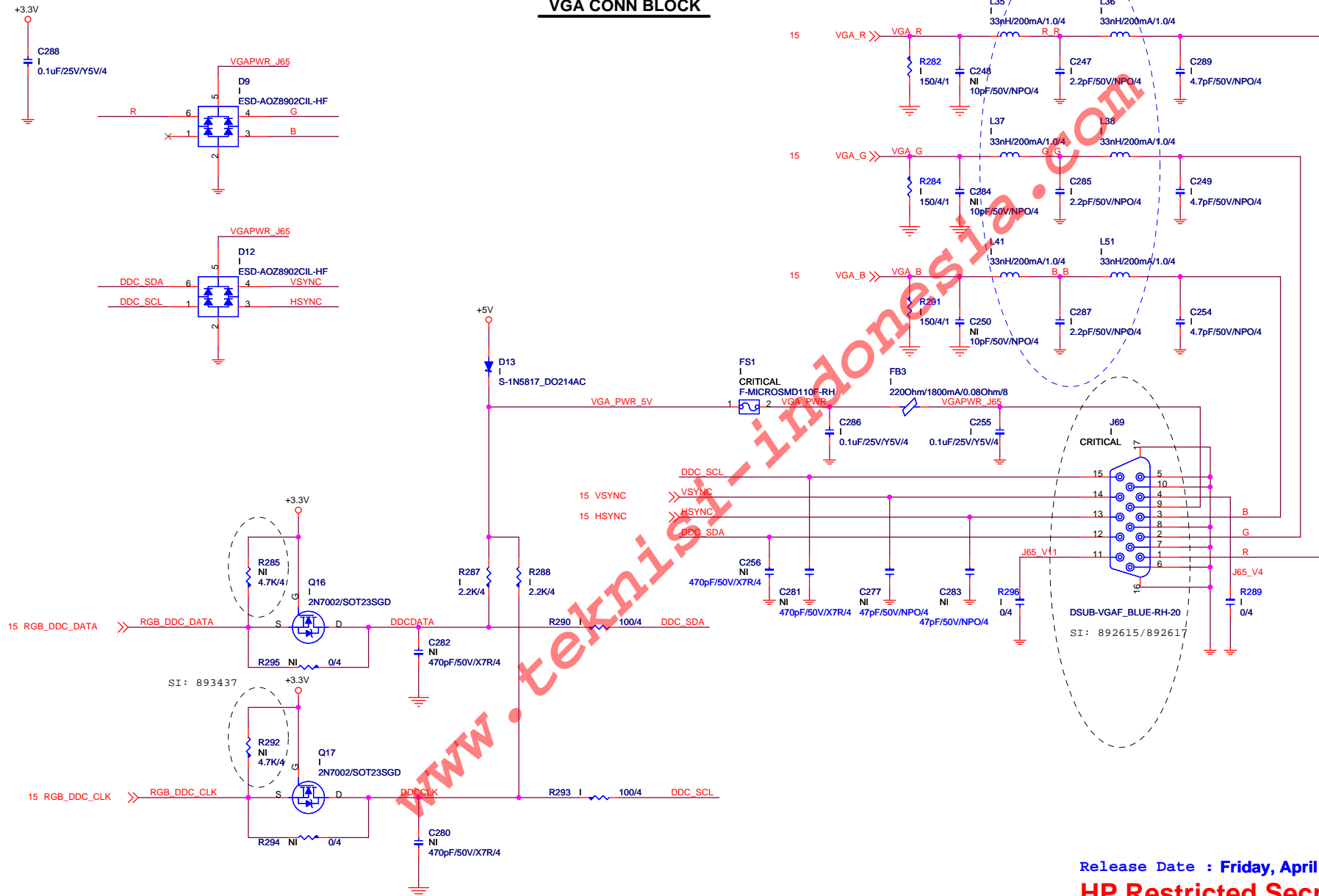


Release Date : Friday, April 25, 2014

HP Restricted Secret

MSI		MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 747866-000(MSI MS-7932)		Rev A	
Size Custom	Document Description	DVI Port CONN	
Date:	Sheet 23 of 59		

VGA CONN BLOCK



Release Date : Friday, April 25, 2014

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MICRO-STAR INT'L CO.,LTD

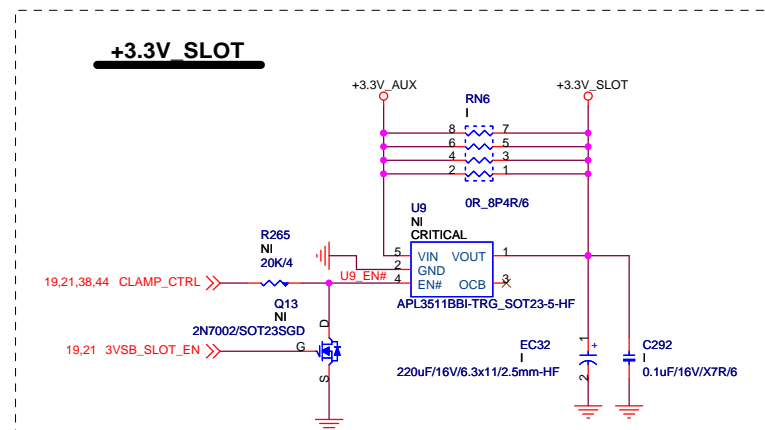
HP SCH P/N: 747866-000(MSI MS-7932)

Size	Document Description
Custom	VGA CONN

	Rev
	A

Date:	Sheet 24 of 59
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SLOT-PCI164P_BLACK-2PITCH-RH-20



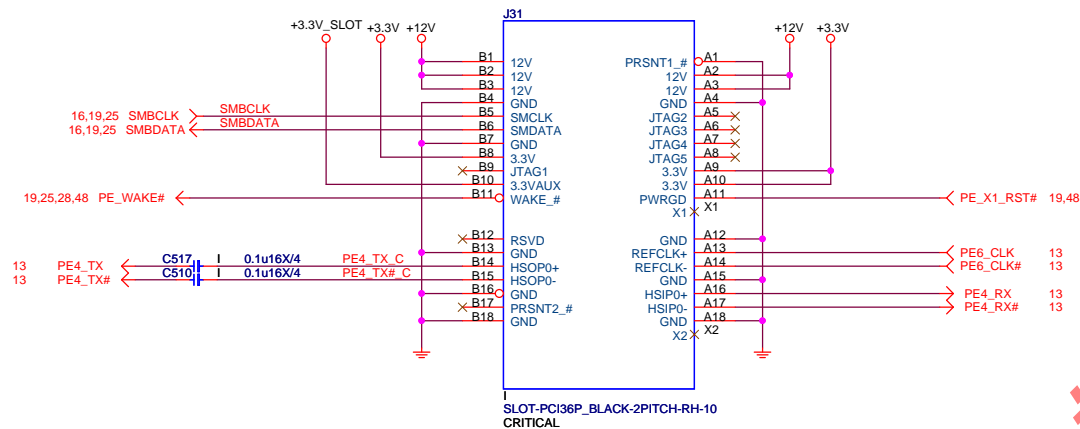
HP Restricted Secret

HP SCH P/N: 747866-000(MSI MS-7932)

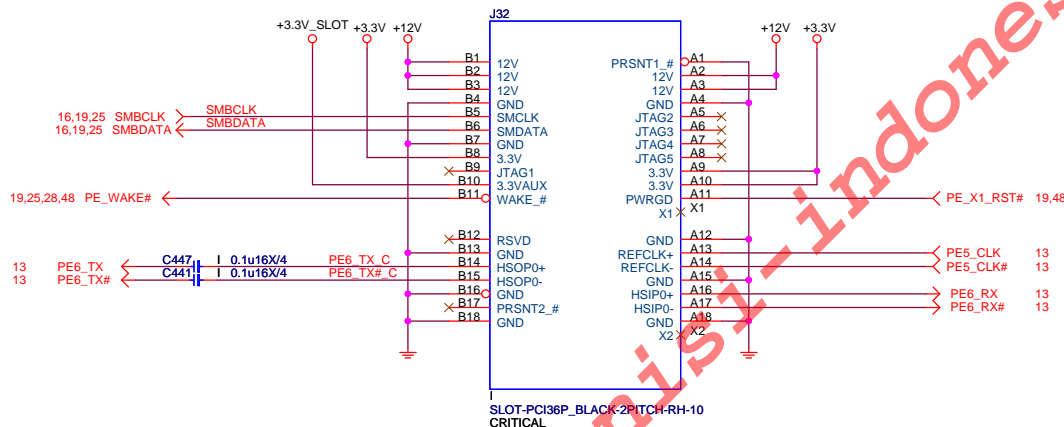
Rev	
A	



PCI EXPRESS x1-PORT




PCI EXPRESS x1-PORT



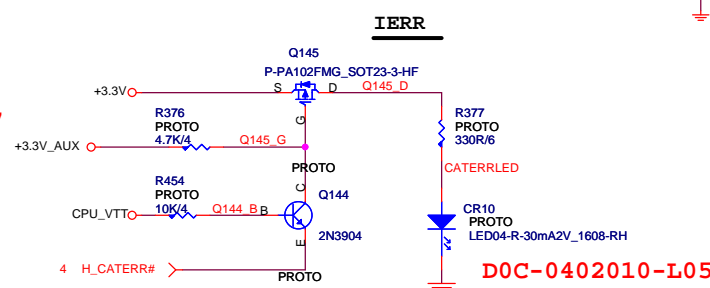
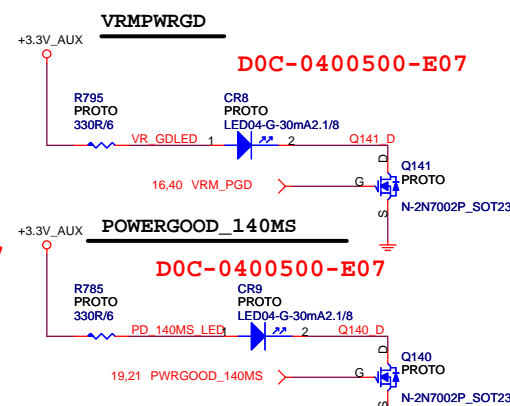
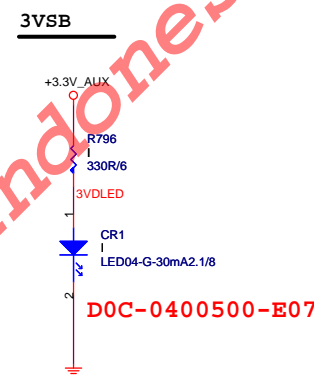
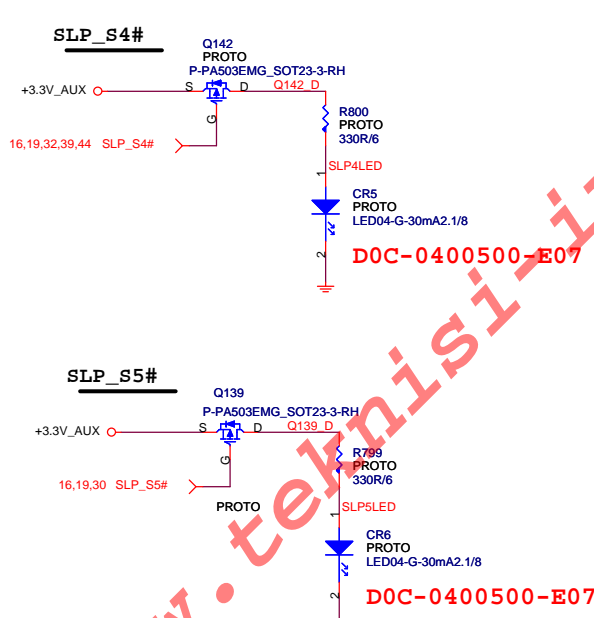
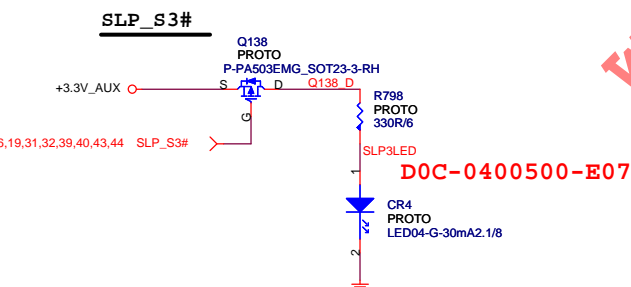
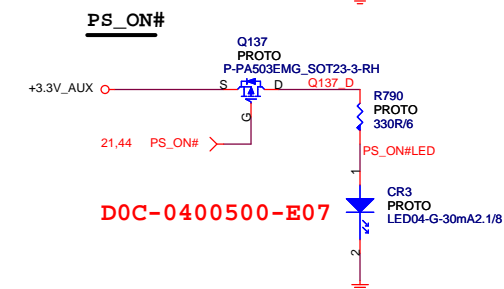
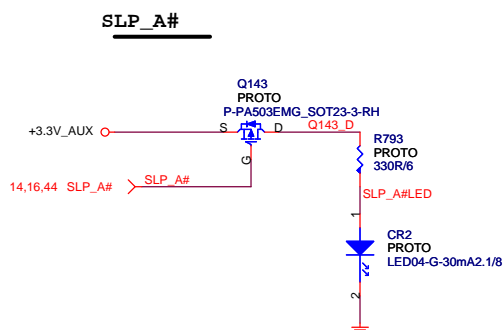
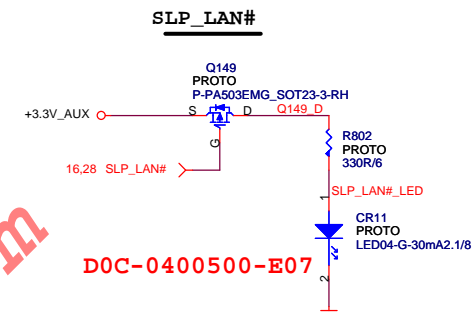
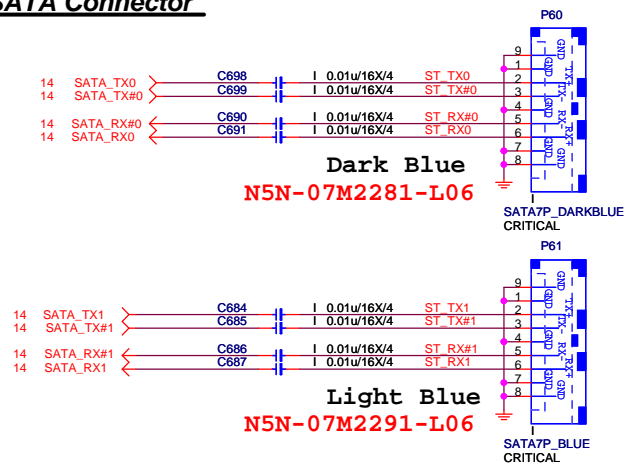
N11-0360381-L06

Release Date : Friday, April 25, 2014

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		MICRO-STAR INT'L CO.,LTD	
HP SCH P/N: 747866-000(MSI MS-7932)		Rev A	
Size Custom	Document Description	PCIE x1 Slots	
Date:	Sheet 26 of 59		

SATA Connector

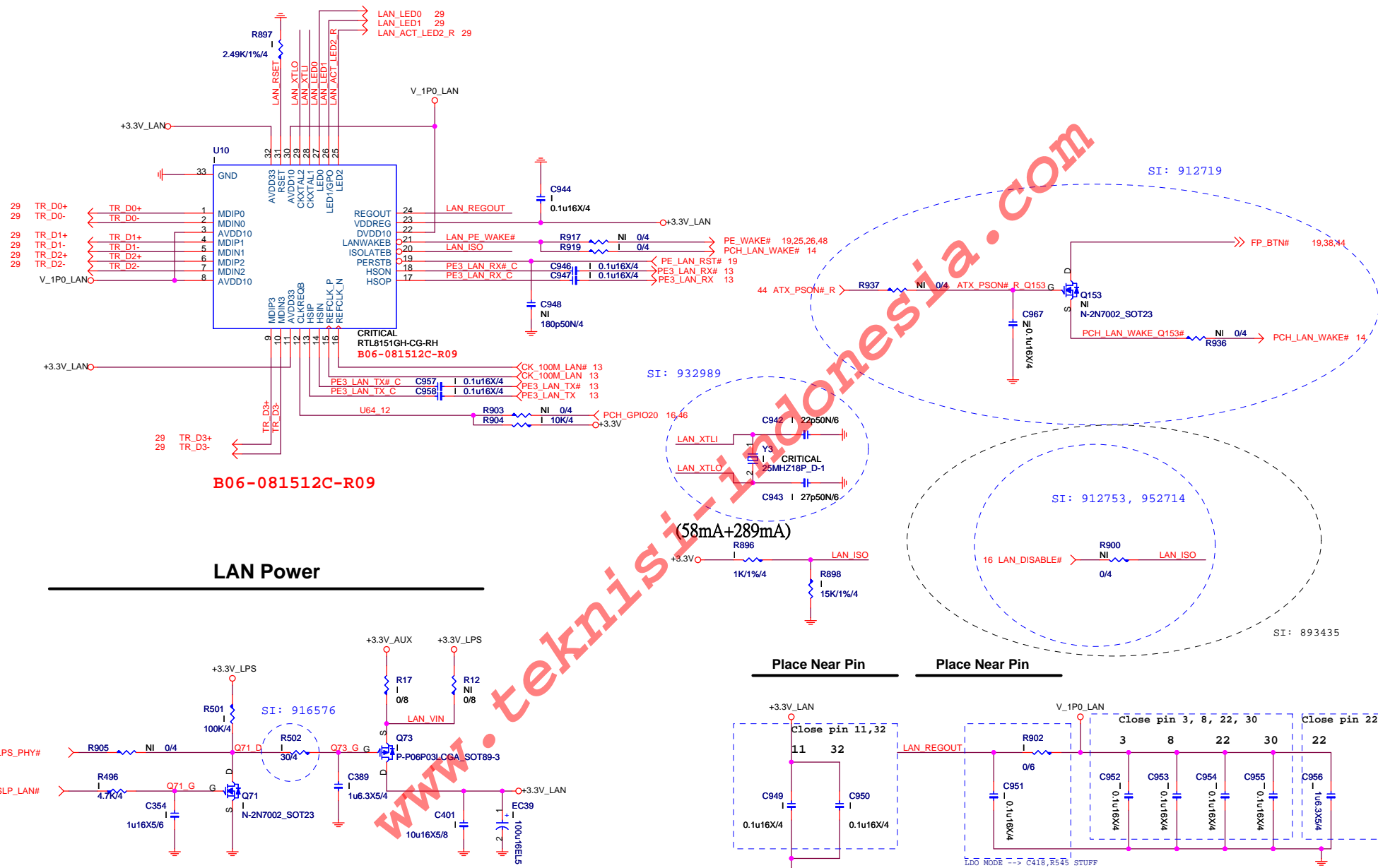


Release Date : Friday, April 25, 2014

HP Restricted Secret

MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 747866-000(MSI MS-7932)		
Size Custom	Document Description	Rev A
SATA/LED		
Date:	Sheet 27	of 59

Gigabit LAN RTL8151GH-CG



Release Date : Friday, April 25, 2014

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MICRO-STAR INT'L CO.,LTD

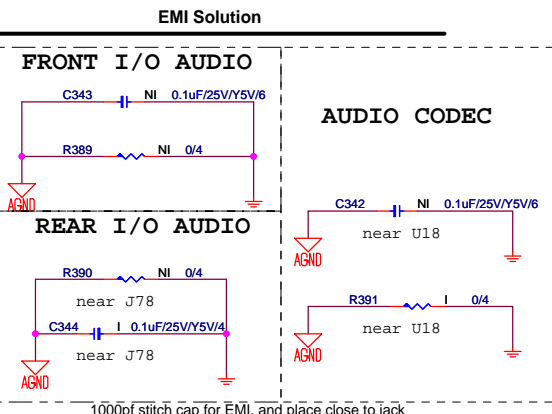
HP SCH P/N: 747866-000(MSI MS-7932)

Size Custom	Document Description Gigabit LAN-RTL8151GH-CG
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Date:	Sheet 28 of 59
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PN:B05-LC2211C-R09



HP Restricted Secret



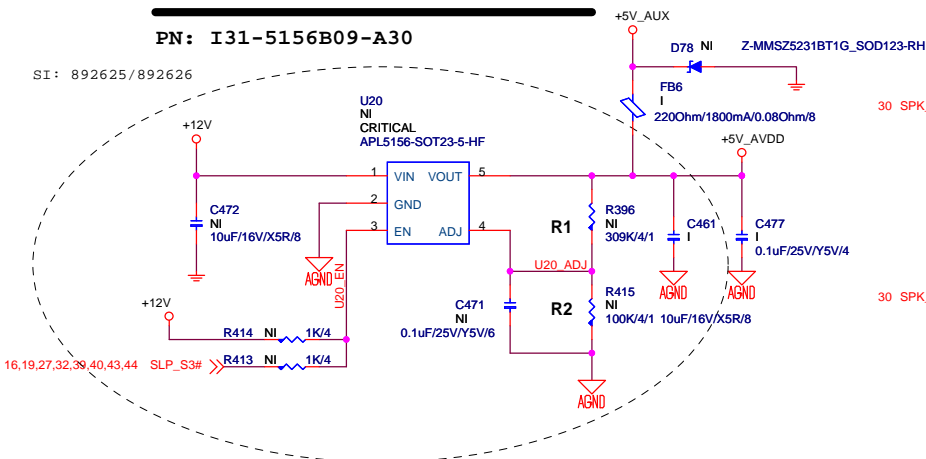
HP SCH P/N: 747866-000(MSI MS-7932)

Size Custom	Document Description Azalia Codec-ALC 221	Rev A
Date:	Sheet 30 of 59	

AUDIO CODEC REGULATORS

PN: I31-5156B09-A30

SI: 892625/892626



SPEAKER HEADER

P/N:N32-1020521-H06

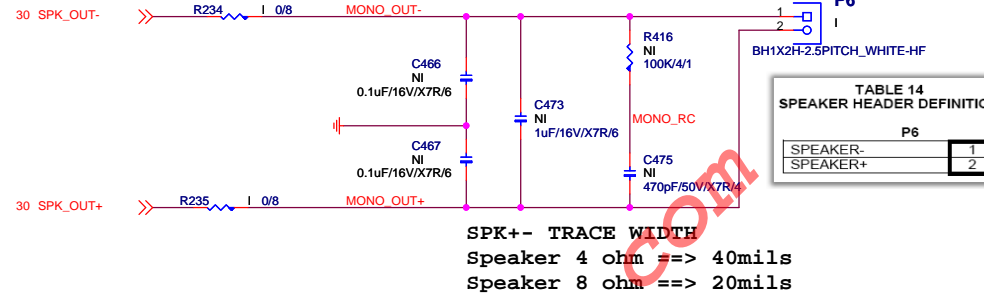
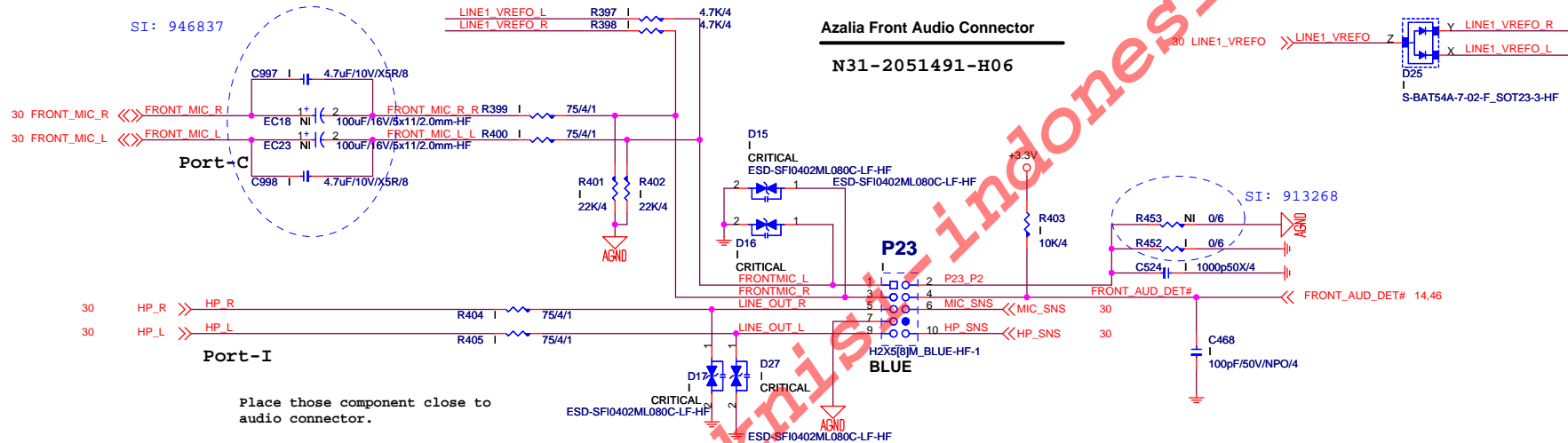


TABLE 14
SPEAKER HEADER DEFINITION

P6	
SPEAKER-	1
SPEAKER+	2

SPK+- TRACE WIDTH
Speaker 4 ohm ==> 40mils
Speaker 8 ohm ==> 20mils

SI: 946837

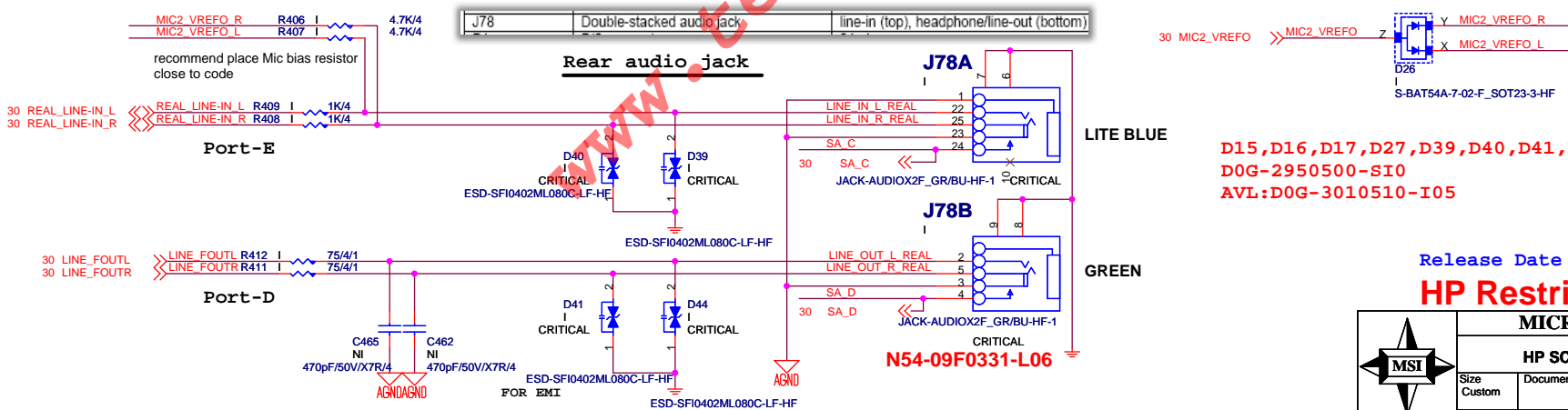


Azalia Front Audio Connector

N31-2051491-H06

Place those component close to audio connector.

Rear audio jack



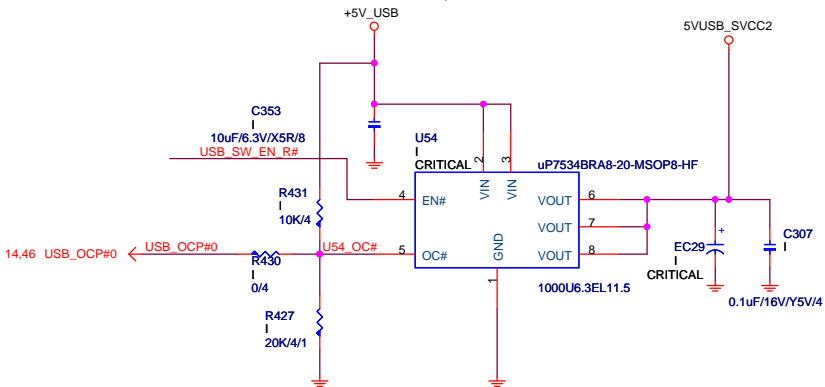
D15, D16, D17, D27, D39, D40, D41, D44
D0G-2950500-SI0
AVL:D0G-3010510-I05

Release Date : Friday, April 25, 2014

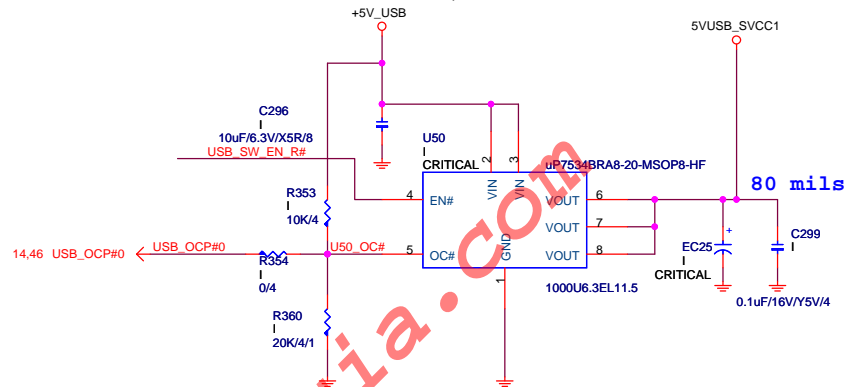
HP Restricted Secret

MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 747866-000(MSI MS-7932)		
Size Custom	Document Description	Rev A
AUDIO CONNECTOR		
Date:	Sheet 31	of 59

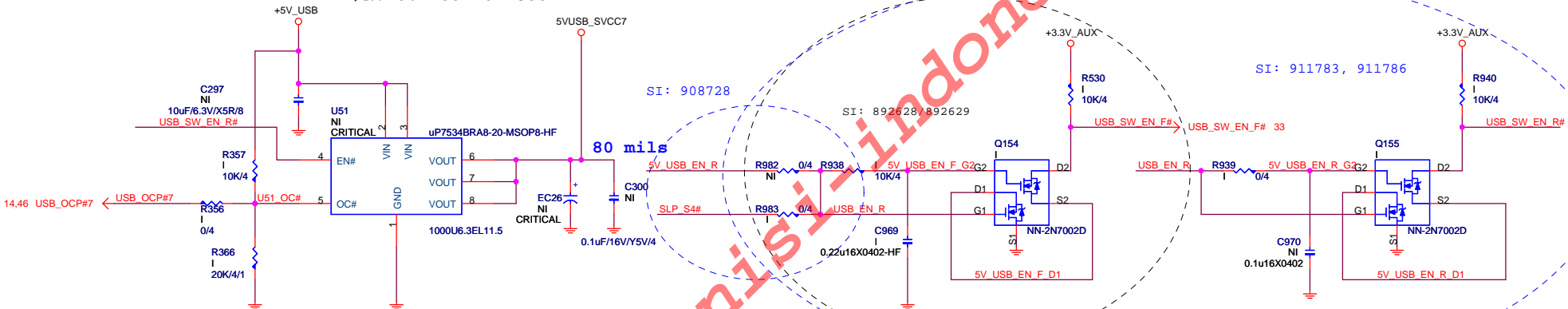
POWER CIRCUIT FOR USB PORT 2,3
P/N: I36-7534B02-U33



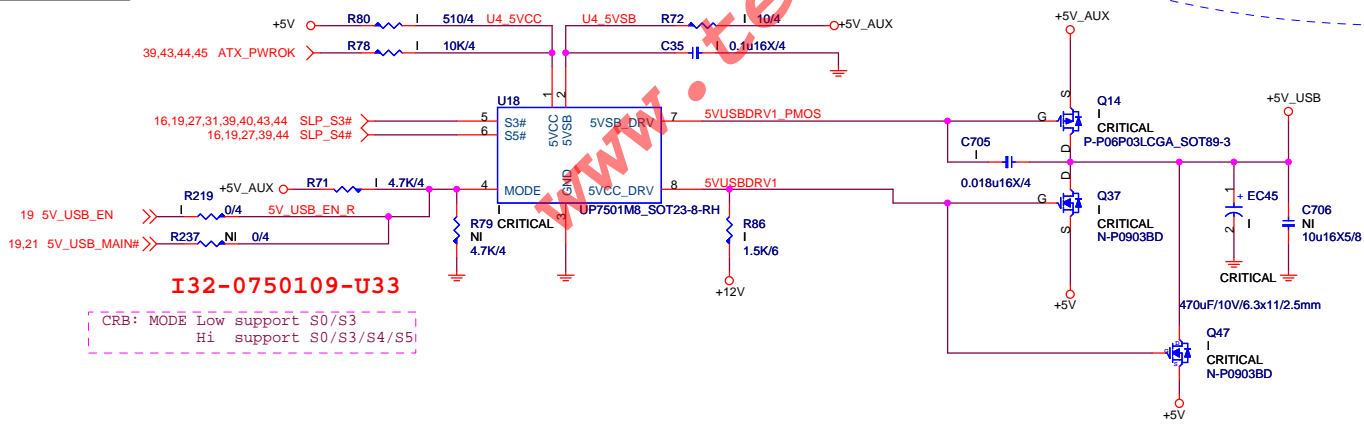
POWER CIRCUIT FOR USB PORT 0,1
P/N: I36-7534B02-U33



POWER CIRCUIT FOR USB PORT 12,13
P/N: I36-7534B02-U33



USB POWER



Release Date : Friday, April 25, 2014

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MICRO-STAR INT'L CO.,LTD

HP SCH P/N: 747866-000(MSI MS-7932)

Size	Document Description
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Rear USB POWER

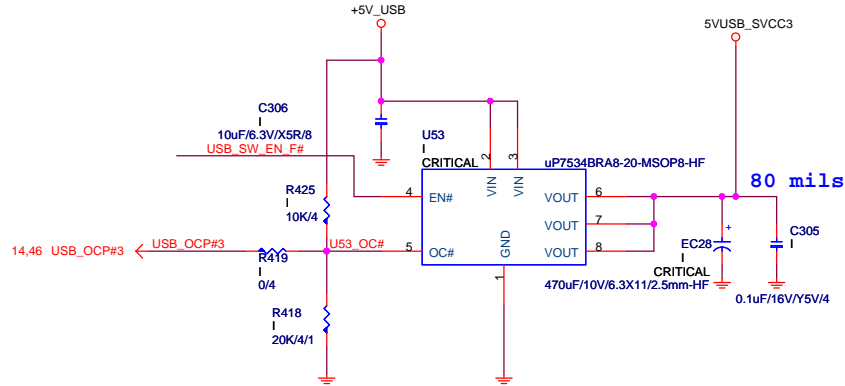
Rev

Date:

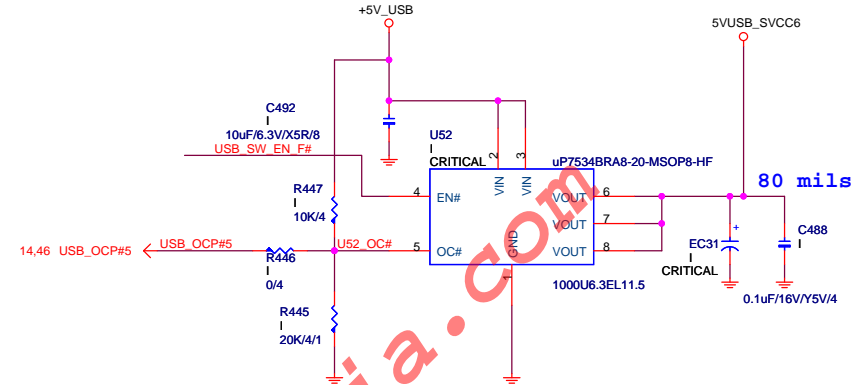
Sheet 32 of 59



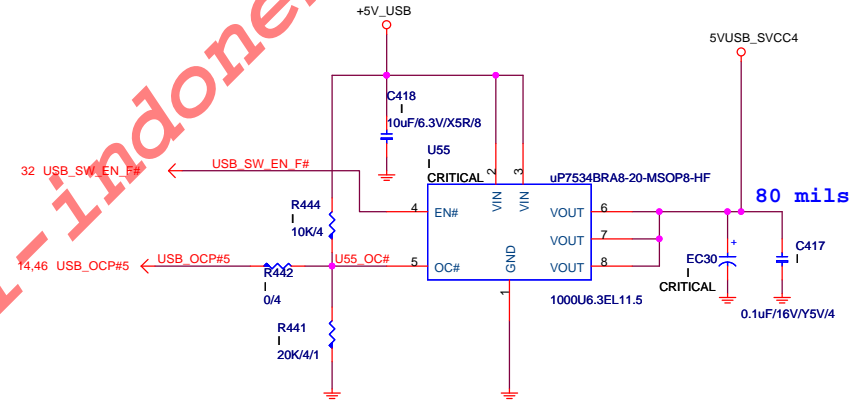
POWER CIRCUIT FOR USB PORT 4,5,6 P/N: I36-7534B02-U33



POWER CIRCUIT FOR USB PORT 10,11 P/N: I36-7534B02-U33



POWER CIRCUIT FOR USB PORT 8,9 P/N: I36-7534B02-U33



Release Date : Friday, April 25, 2014

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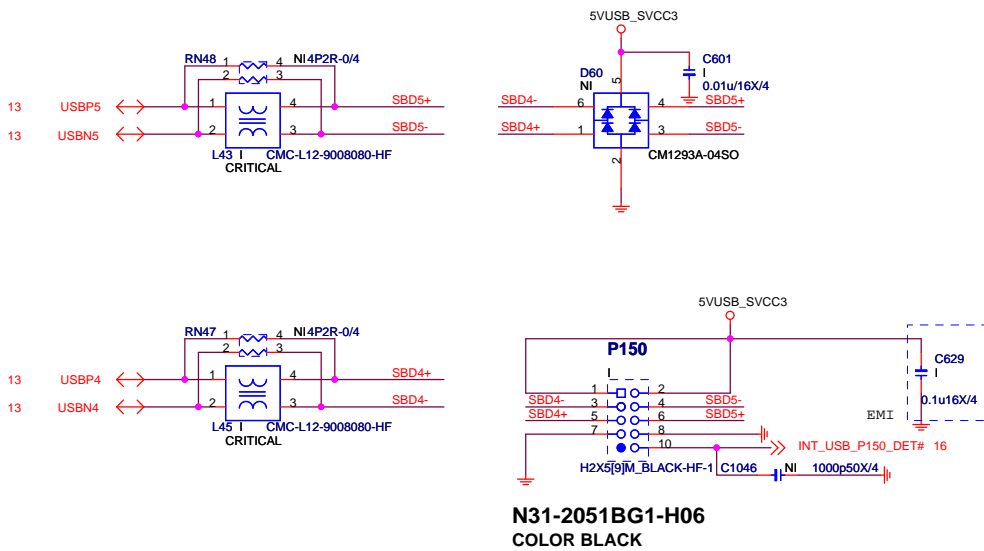


MICRO-STAR INT'L CO.,LTD

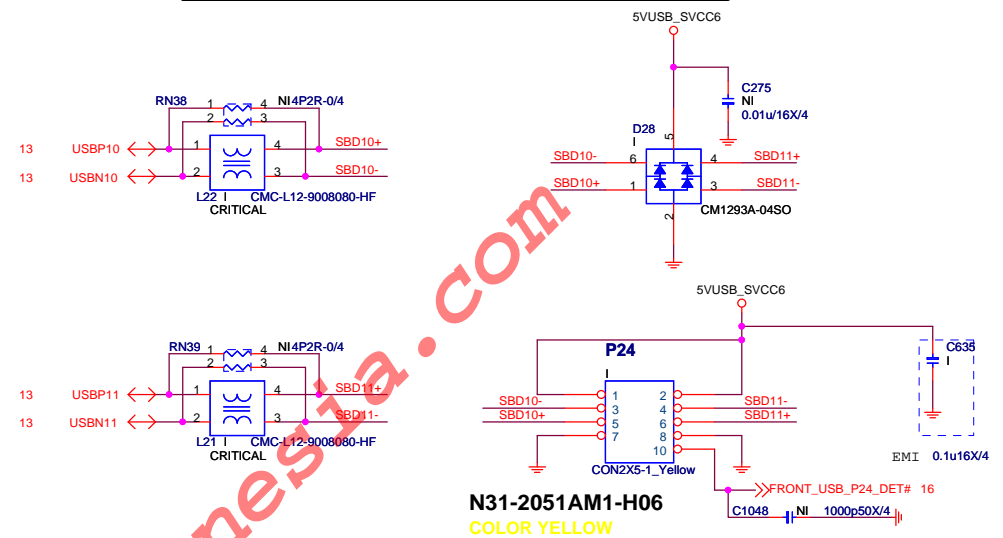
HP SCH P/N: 747866-000(MSI MS-7932)

Size	Document Description	Rev
Custom	Front USB POWER	A
Date:	Sheet 33 of 59	

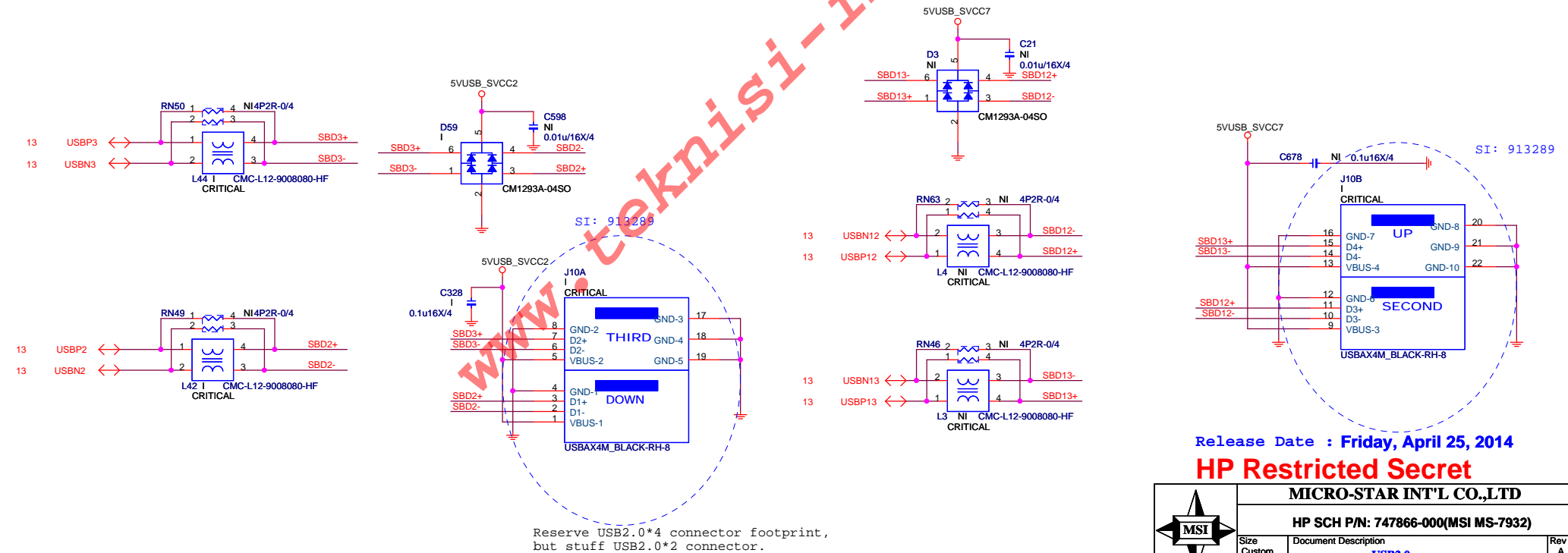
Internal USB Connector For USB Port 4 / 5



Front Panel USB Connector For USB Port 10 / 11



Rear USB Connector For USB Port 2/3



Release Date : Friday, April 25, 2014

HP Restricted Secret

MICRO-STAR INT'L CO.,LTD

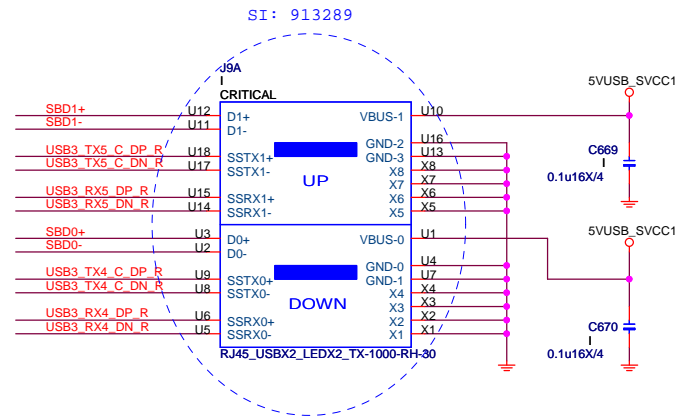
HP SCH P/N: 747866-000(MSI MS-7932)

USB2.0

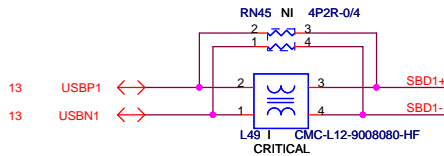
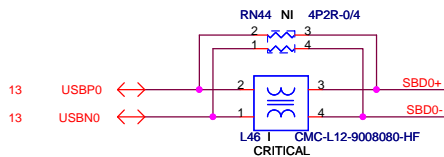
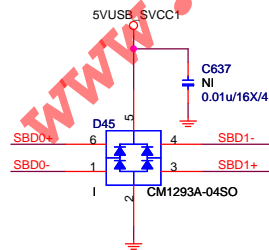
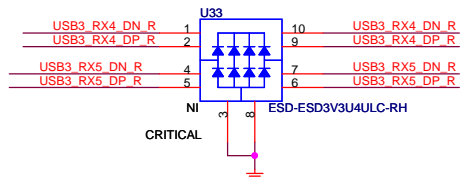
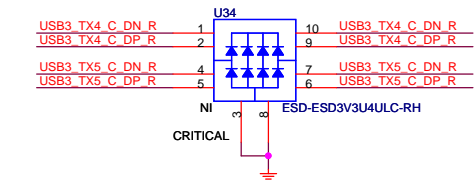
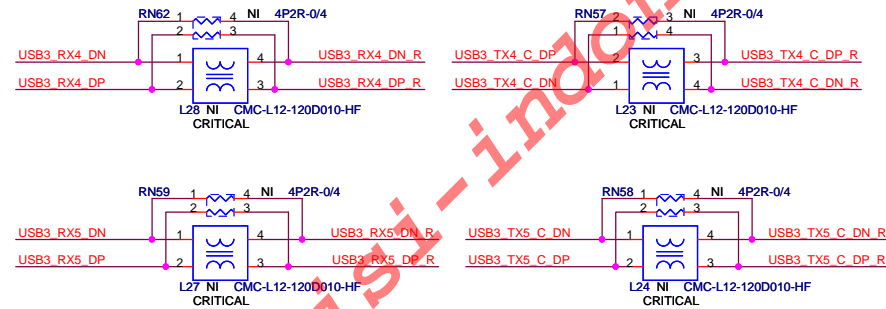
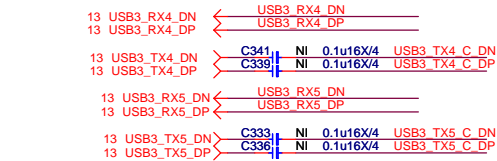
Rev
A



Size	Document Description	Rev
Custom	USB2.0	A
Date:		



REAR USB3.0 Connector For USB3.0 Port 4/5

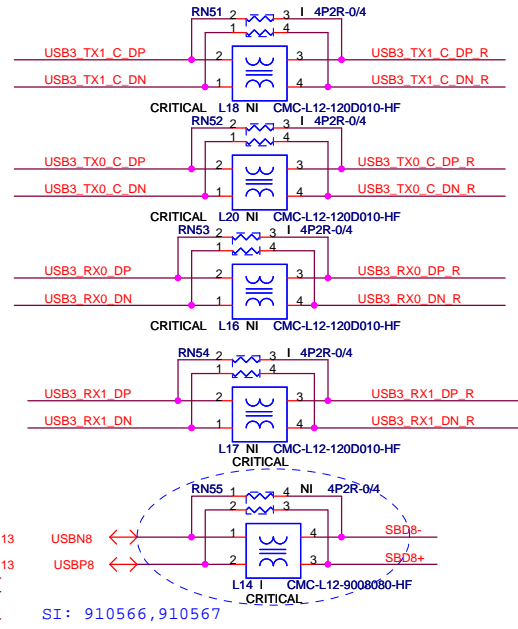
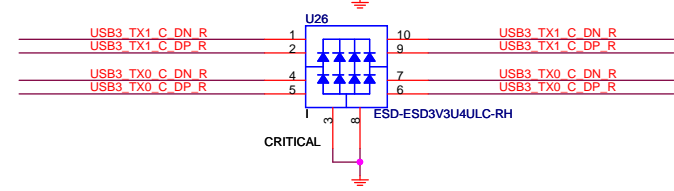
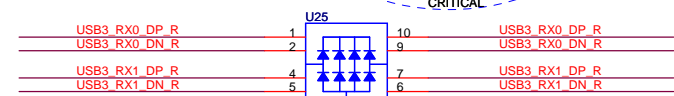
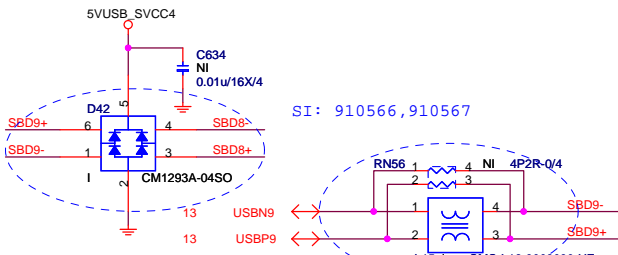
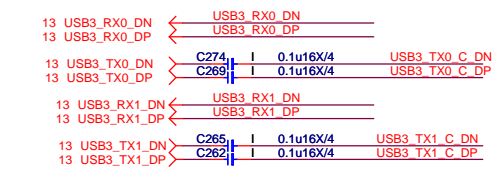


Release Date : Friday, April 25, 2014

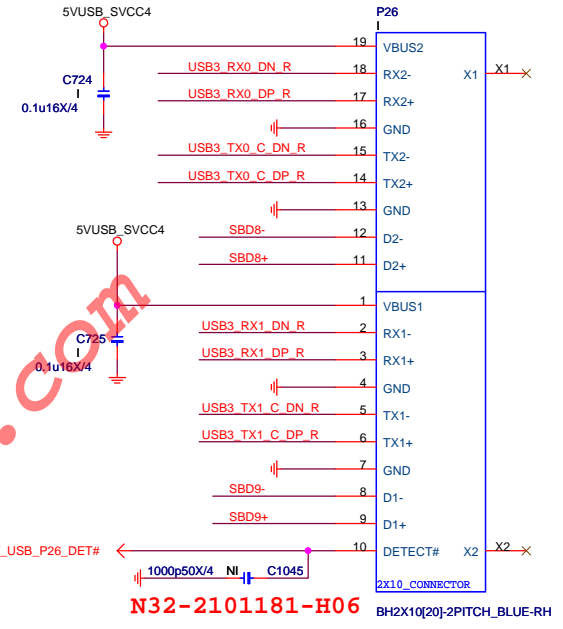
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MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 747866-000(MSI MS-7932)		
Size	Document Description	Rev
Custom	Rear USB 3.0	A
Date:	Sheet	35 of 59

FRONT USB3.0 Connector For USB3.0 Port 1 / 2



The six USB 3.0 pairs can be mapped with any USB 2.0 pair to a given connector but ACPI tables and BIOS should be updated to reflect the USB 2.0 to USB 3.0 pair mapping., DG PAGE 159

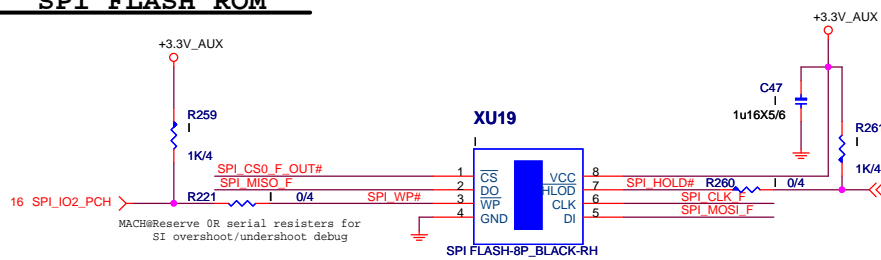


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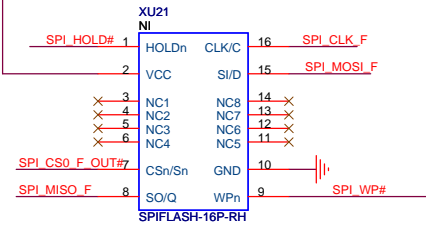
Release Date : Friday, April 25, 2014
HP Restricted Secret

	MICRO-STAR INT'L CO.,LTD			
	HP SCH P/N: 747866-000(MSI MS-7932)			
	Size Custom	Document Description		Rev A
	Front USB 3.0			
Date:		Sheet 36	of 59	

SPI FLASH ROM



SPI 64M ROM1



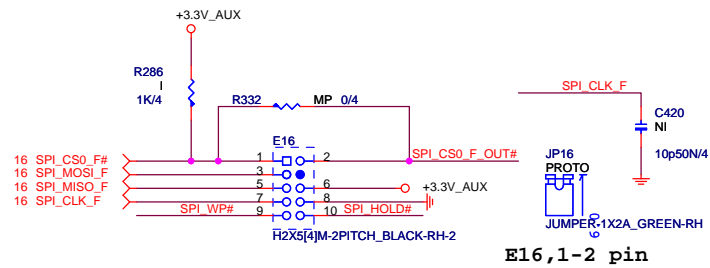
PN:N14-0160010-L06

BIOS



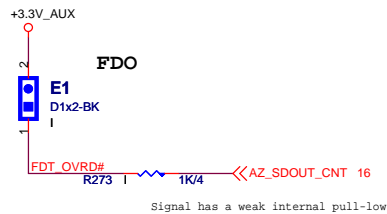
M31-25Q6443-W03

SPI DEBUG PROT



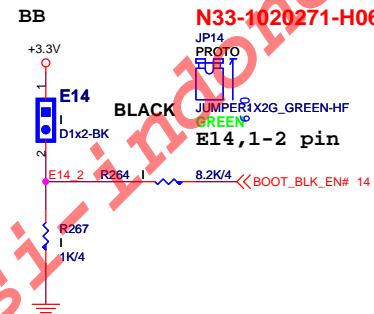
Flash Descriptor Override Header (ME_DIS)

FLASH DESCRIPTOR OVERRIDE

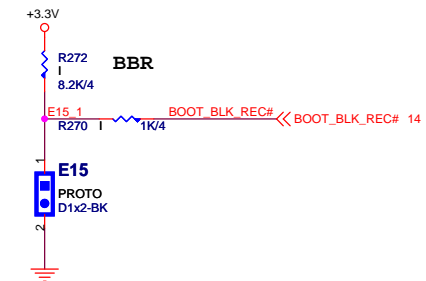


N31-1020151-H06

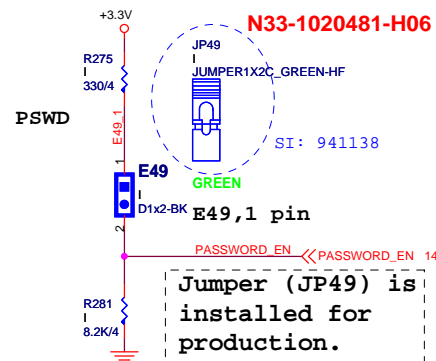
BOOT BLOCK WRITE JUMPER



BOOT BLOCK RECOVERY HEADER



PASSWORD JUMPER



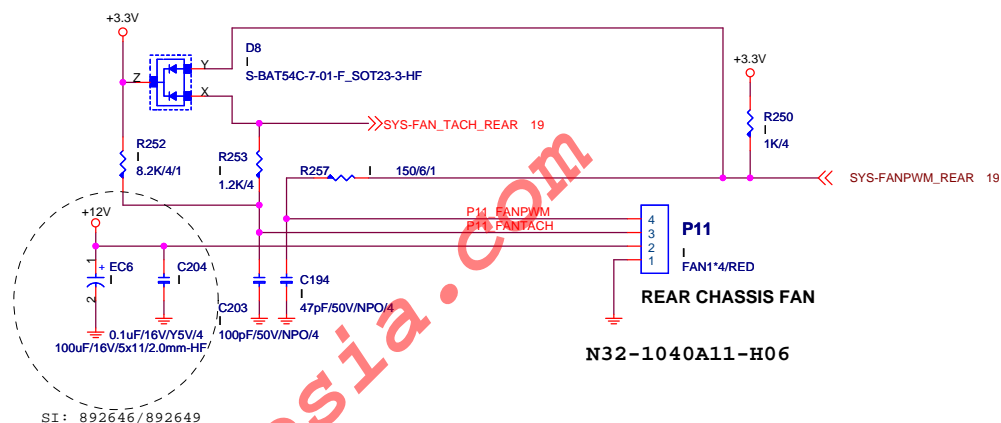
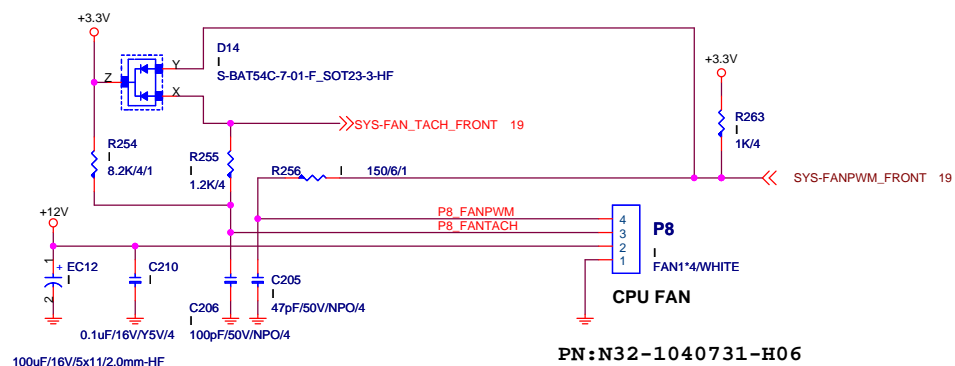
Release Date : Friday, April 25, 2014

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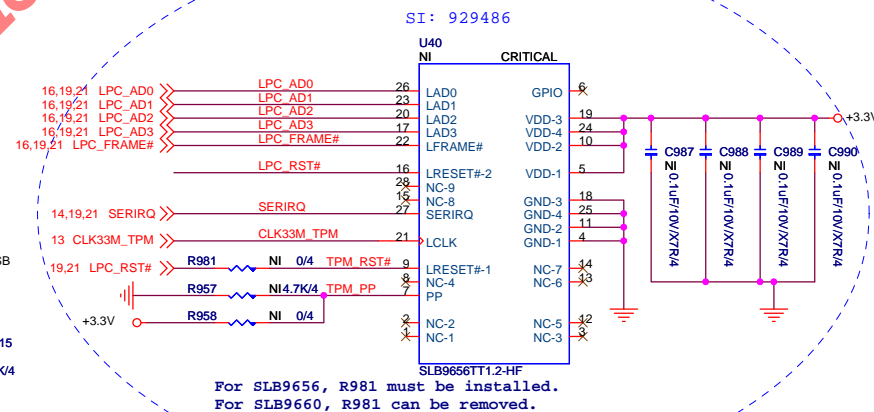
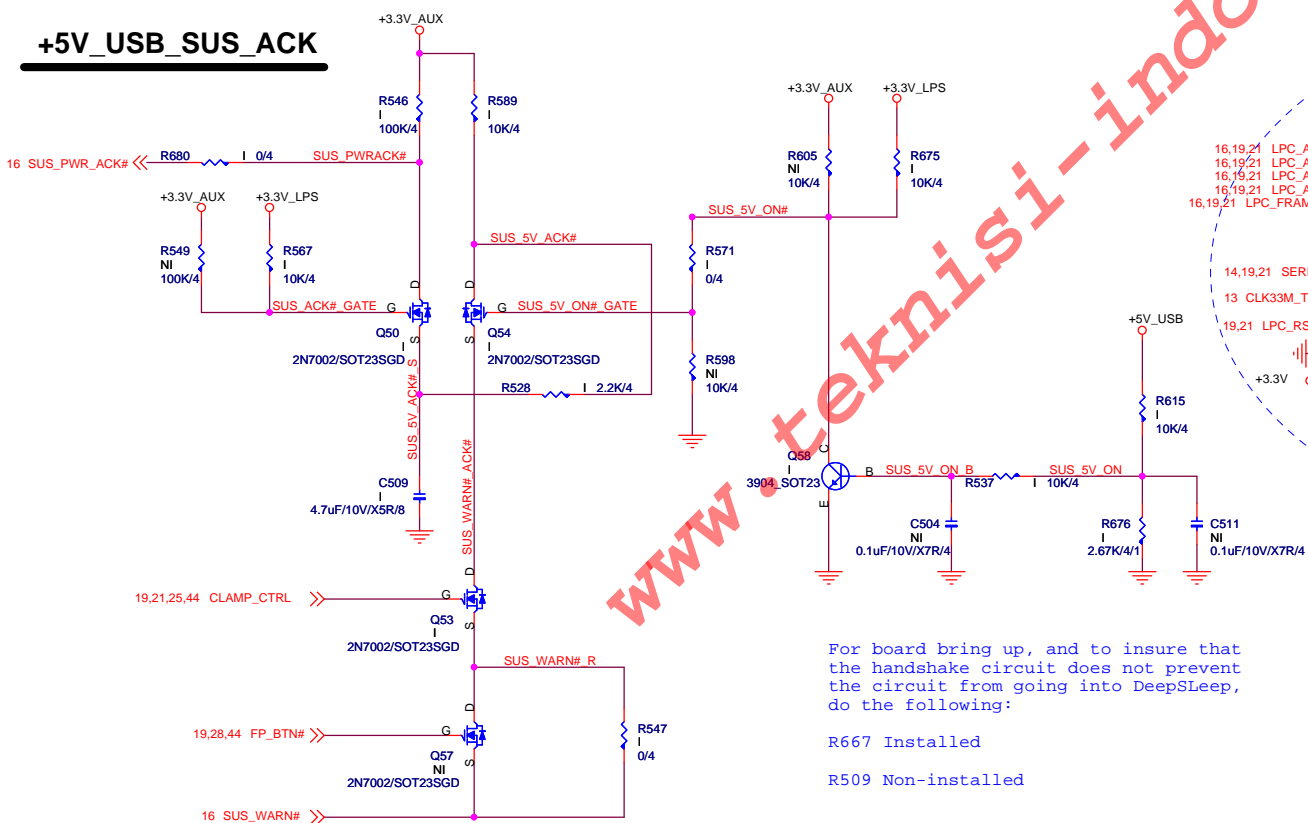


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Size Custom	Document Description Header/ SPI		Rev A
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FAN BLOCK



+5V_USB_SUS_ACK



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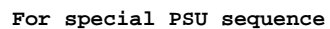
MICRO-STAR INT'L CO.,LTD

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$$V_{out} = 0.8[(R_{251} + R_{246}) / R_{251}]$$


0.75V - 1.1A - 0.825W



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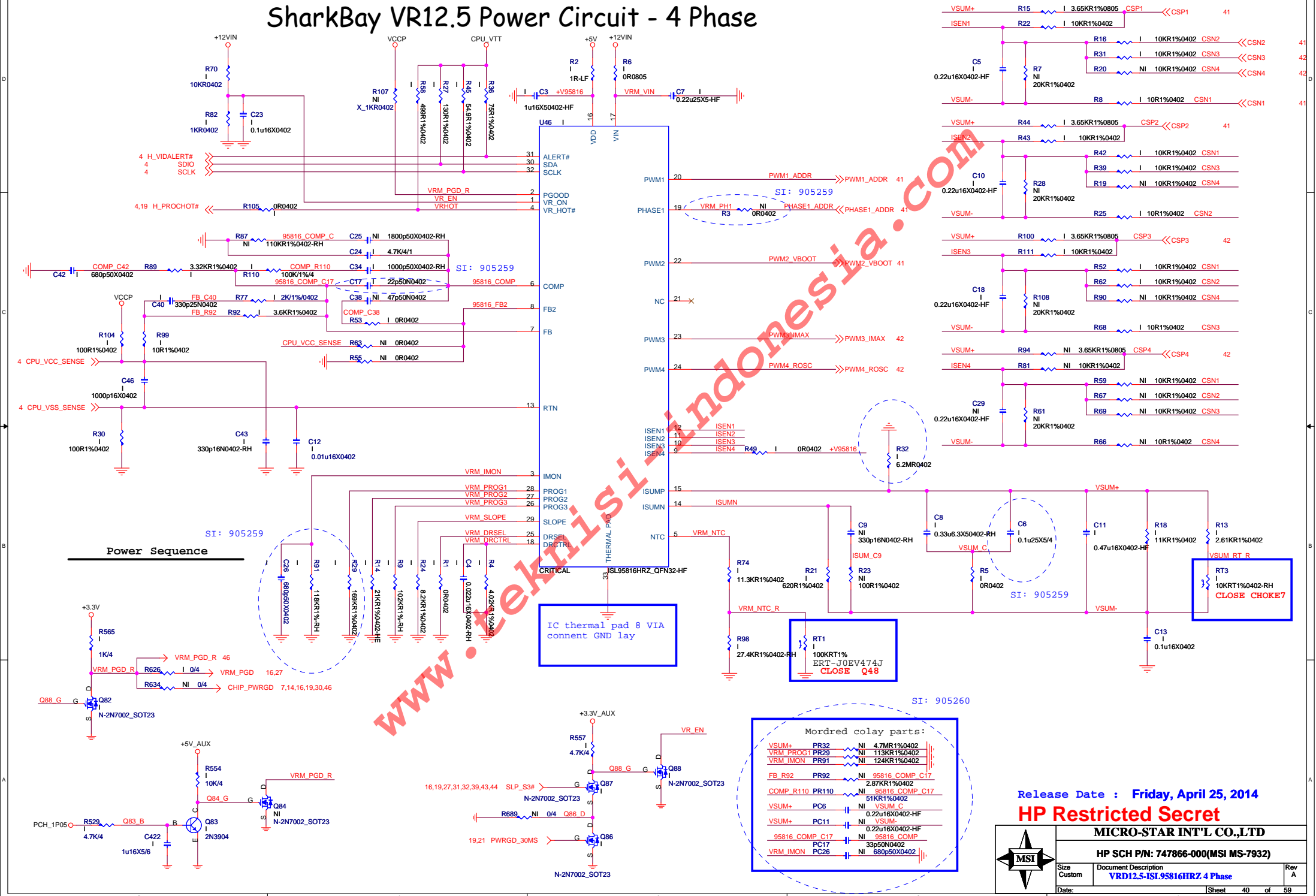
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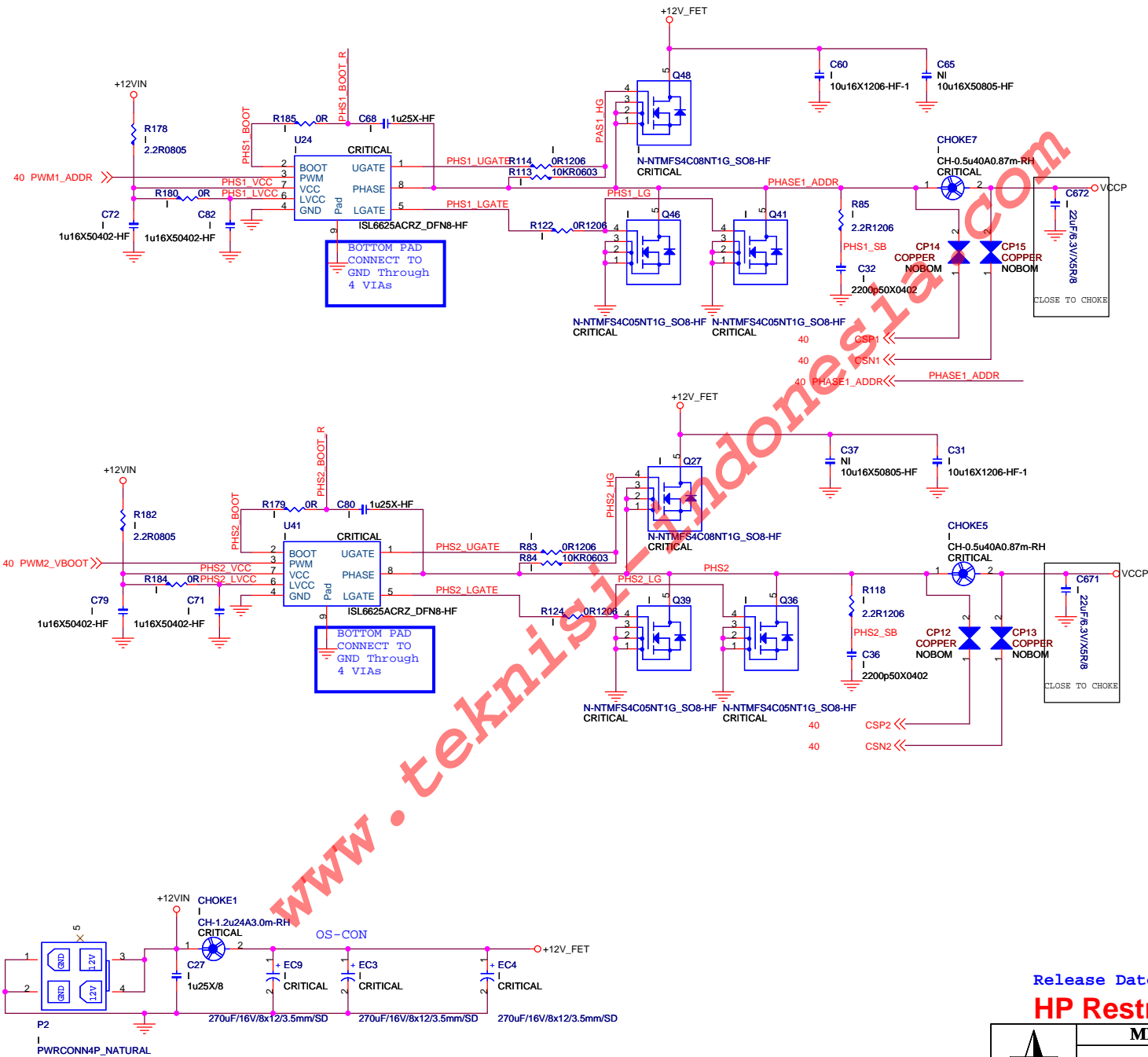
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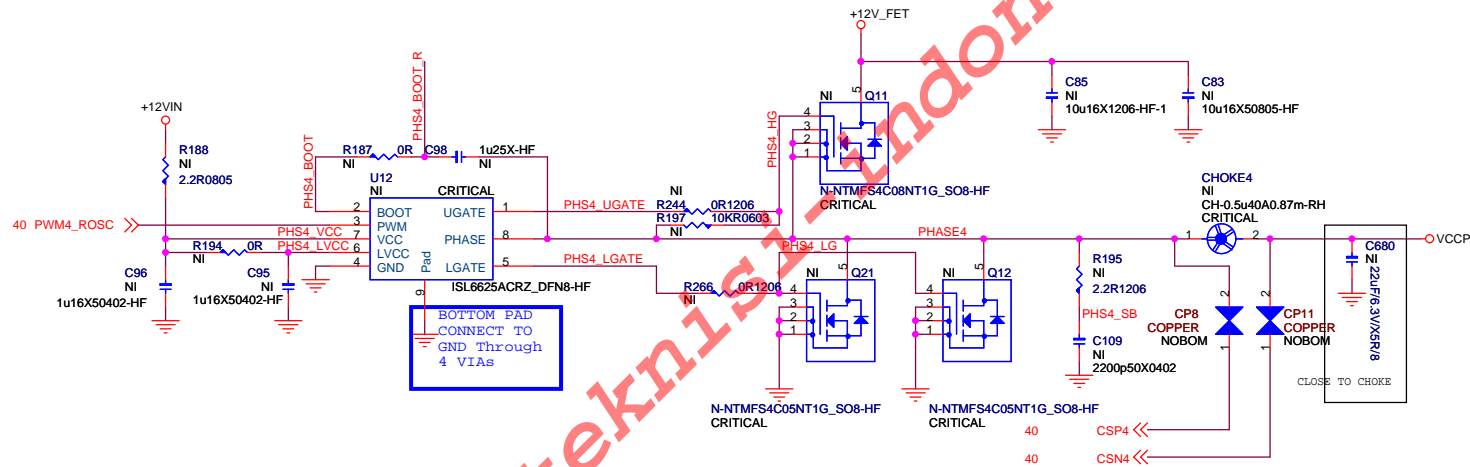
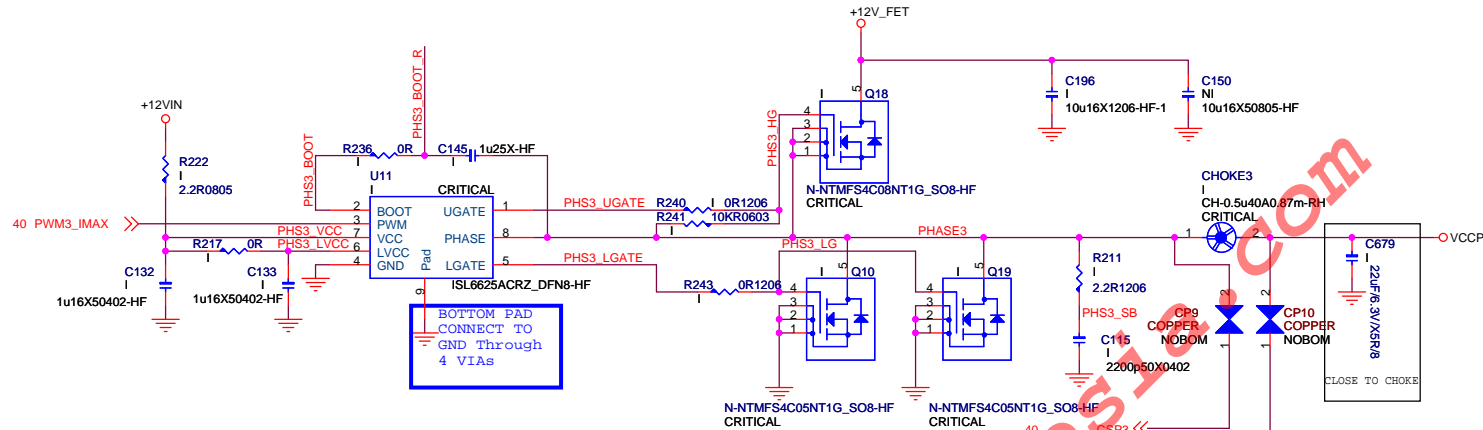
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Custom	DDR Power

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SharkBay VR12.5 Power Circuit - 4 Phase







C71-5610611-N07

SI: 893441

Ceramic / 0805/X5R

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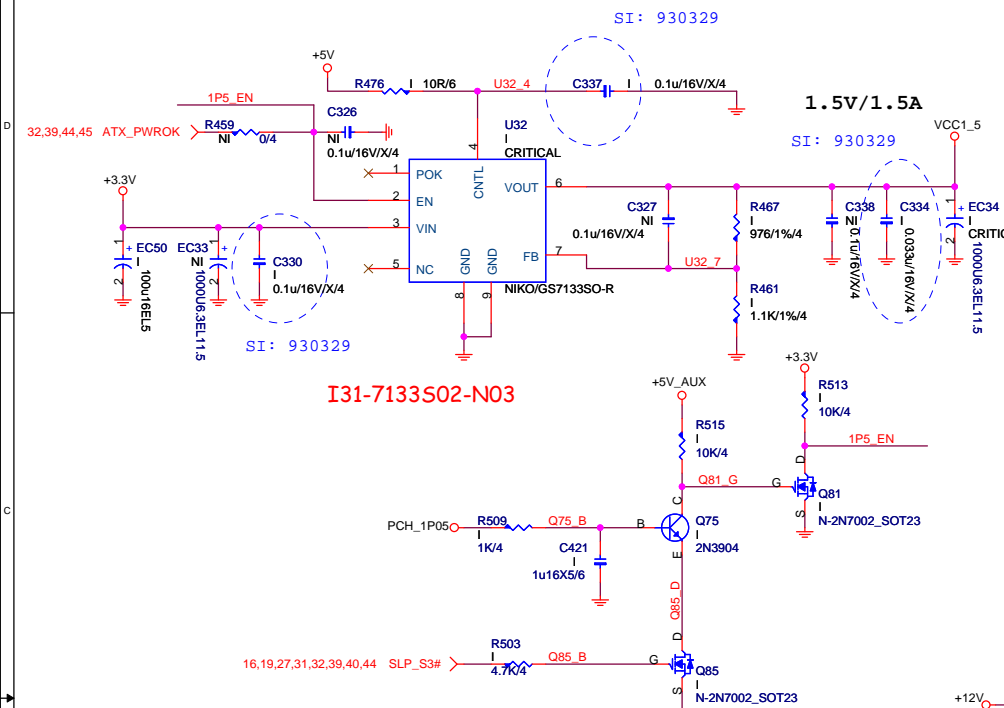
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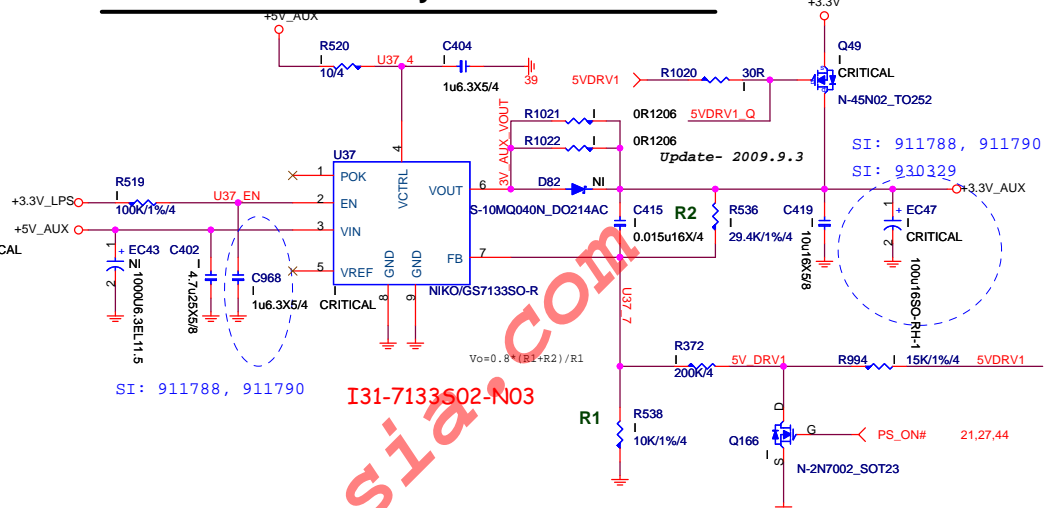
Rev A

Date: Sheet 42 of 59

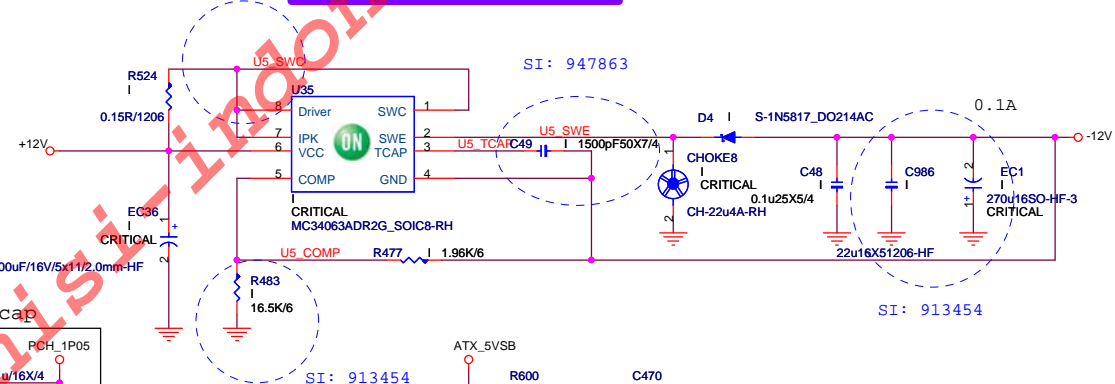
1.5V Power



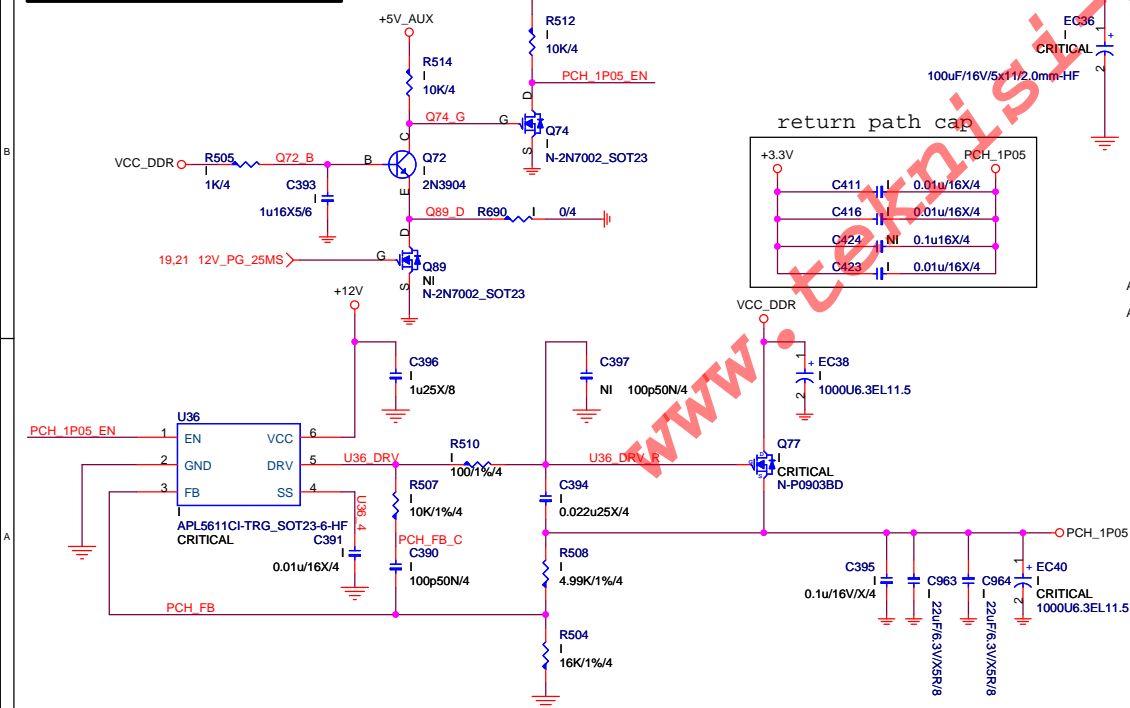
3V Standby Power



-12V POWER



PCH Core Power Control



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MICRO-STAR INT'L CO.,LTD

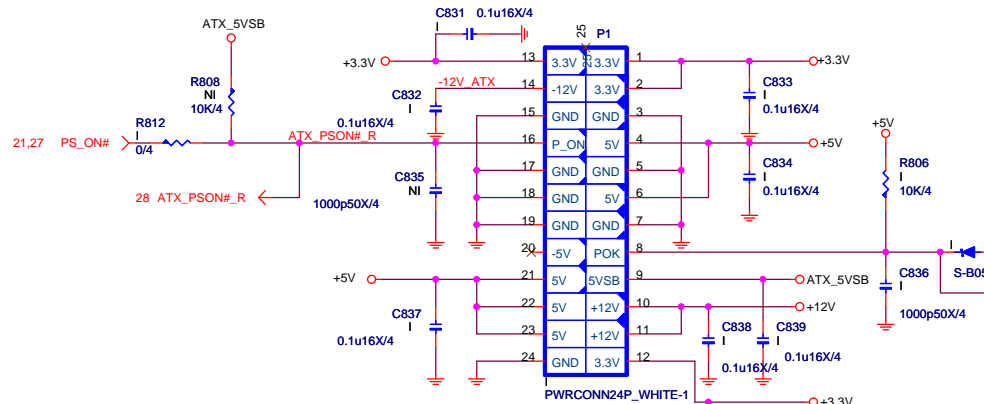
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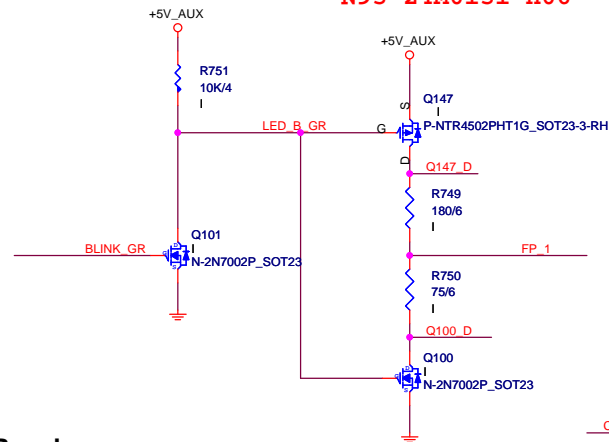
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ATX Power Connector / Front Panel / LED/DSW

ATX CONNECTOR

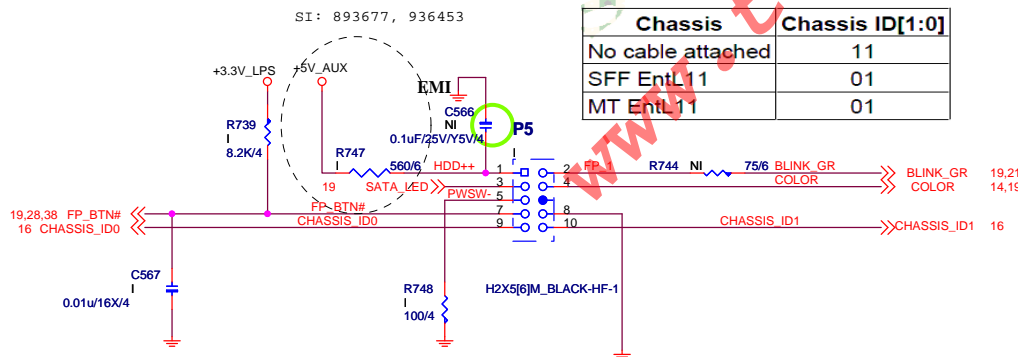


N93-24M0131-H06



Front Panel

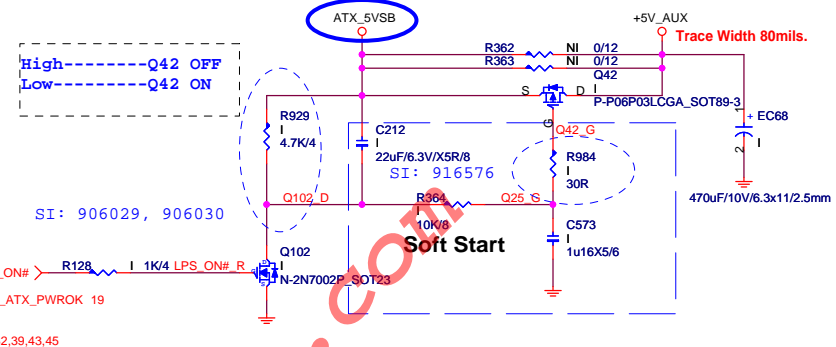
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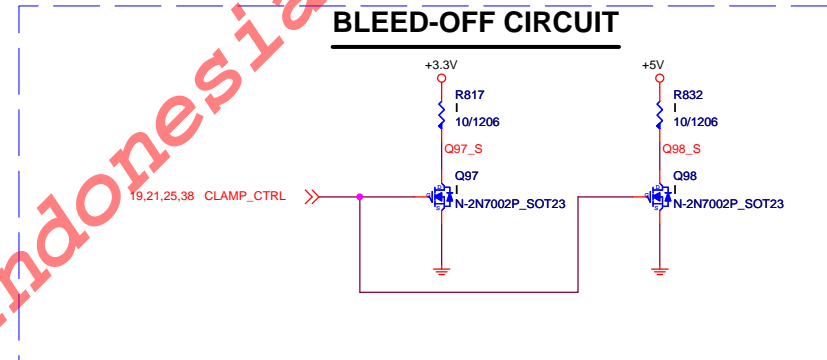
CHASSIS ID[1:0]

Chassis	Chassis ID[1:0]
No cable attached	11
SFF EntL11	01
MT EntL11	01

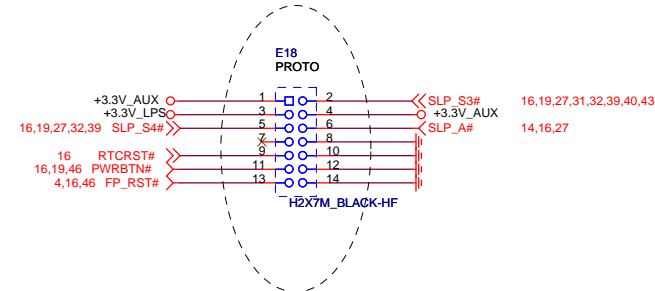
+5V AUX Power Switch Tune ATX_5VSB inrush current to 2A from 4A



BLEED-OFF CIRCUIT



SI: 892659/892663



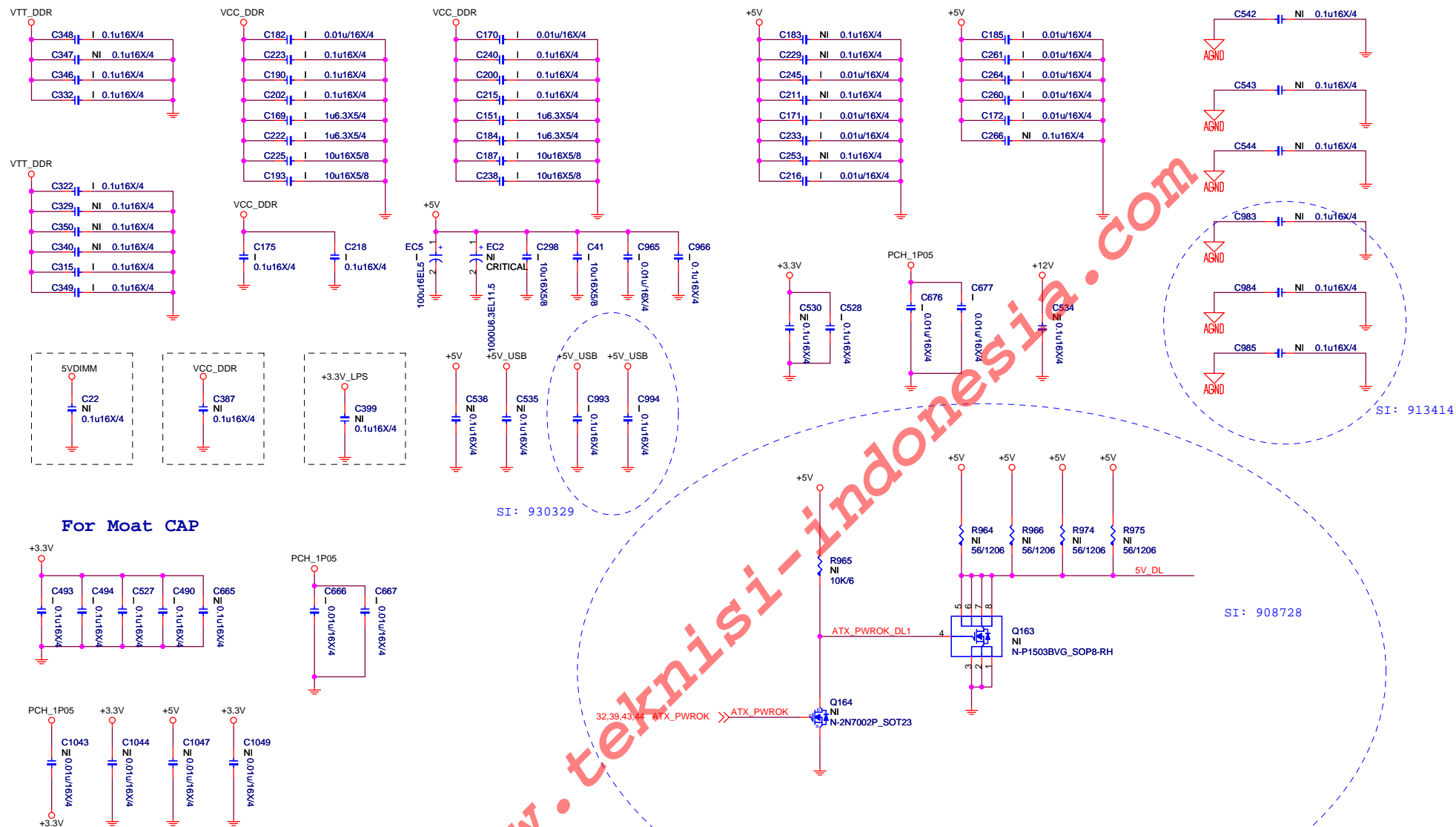
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Size Custom	Document Description
ATX/F_Panel/EMI	
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EMI CAPs



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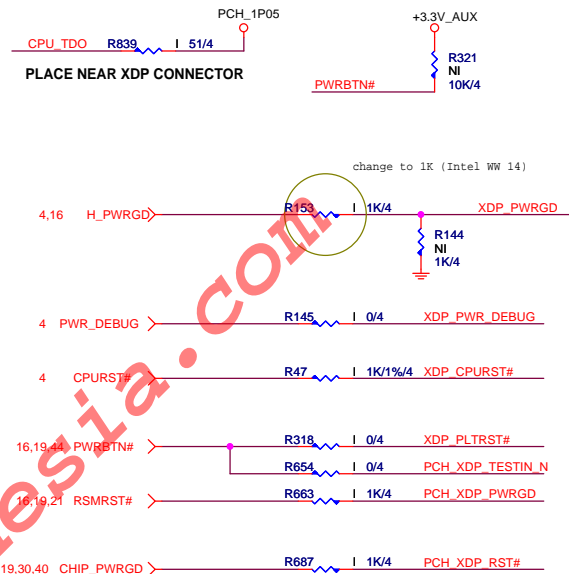
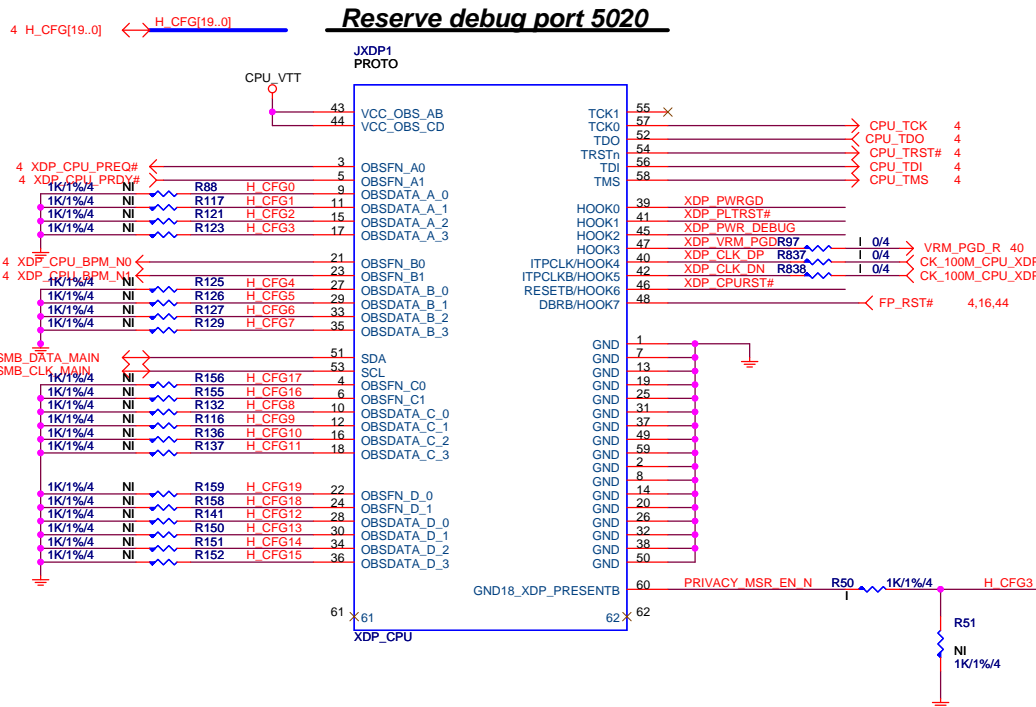
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HP SCH P/N: 747866-000(MSI MS-7932)

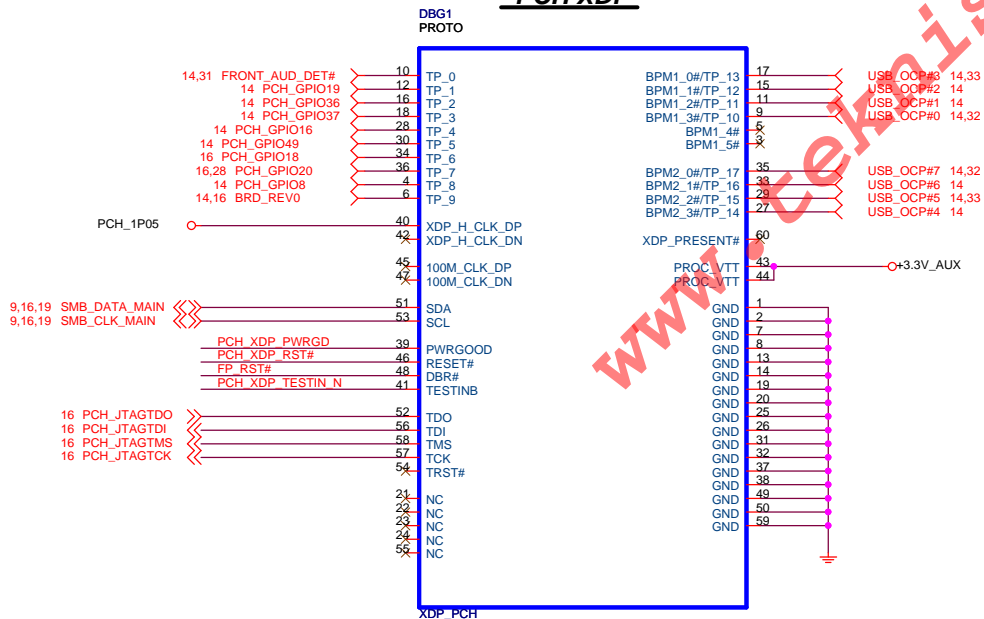
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Rev A

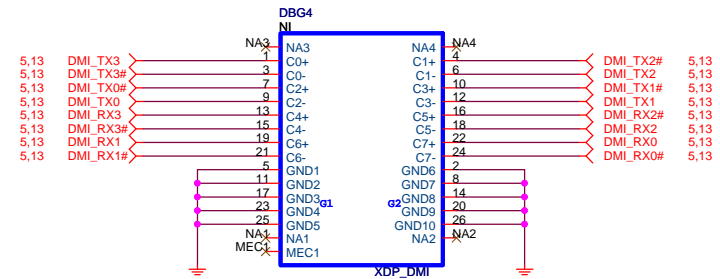
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PCH XDP



DMI XDP

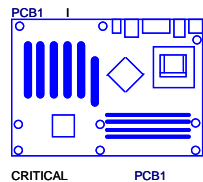


Release Date : Friday, April 25, 2014

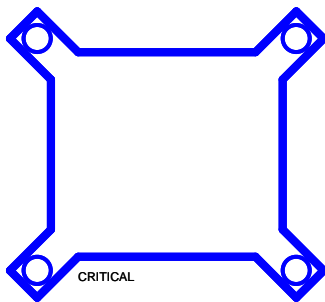
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MICRO-STAR INT'L CO.,LTD		
HP SCH P/N: 747866-000(MSI MS-7932)		
Size Custom	Document Description	Rev A
CPU/PCH/DMI XDP		
Date:	Sheet 46 of 59	

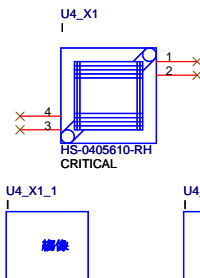
Manual Parts



XU1_X2
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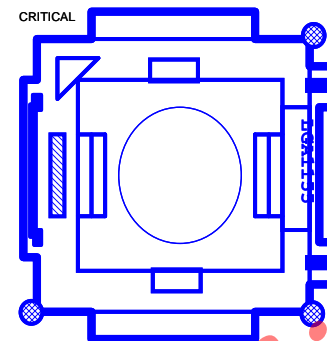


E93-0000099-A21
AVL:E22-B009010-C22



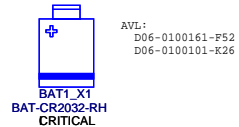
XU1_X1
CPU SOCKET

CRITICAL



E21-AC71010-L06
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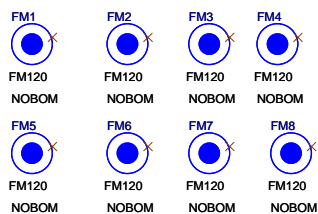
Simulation



AVL:
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D06-0100101-K26

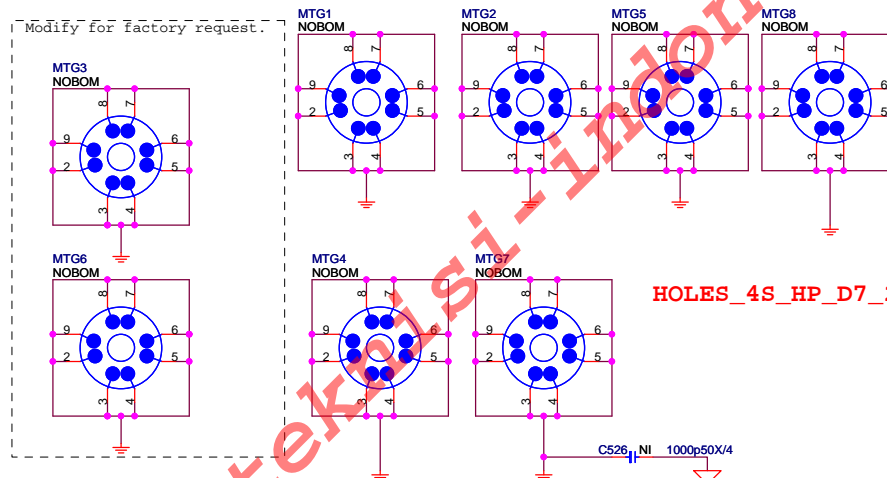
D06-0100101-P01

Optics Orientation Holes



Mounting Holes

Modify for factory request.



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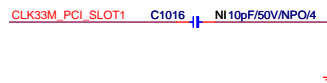
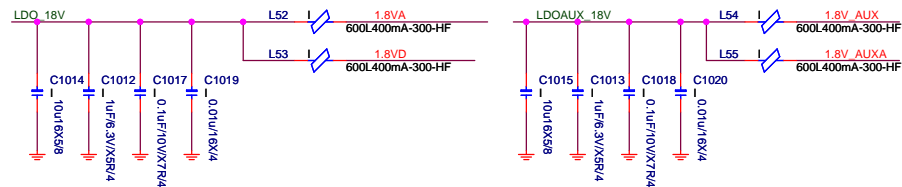
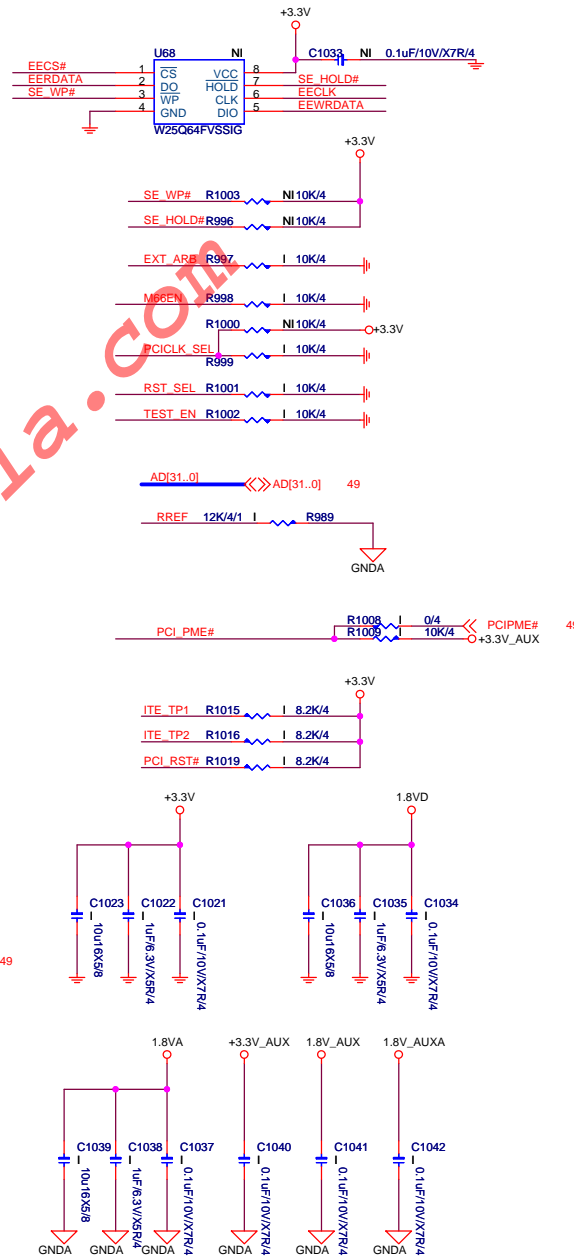
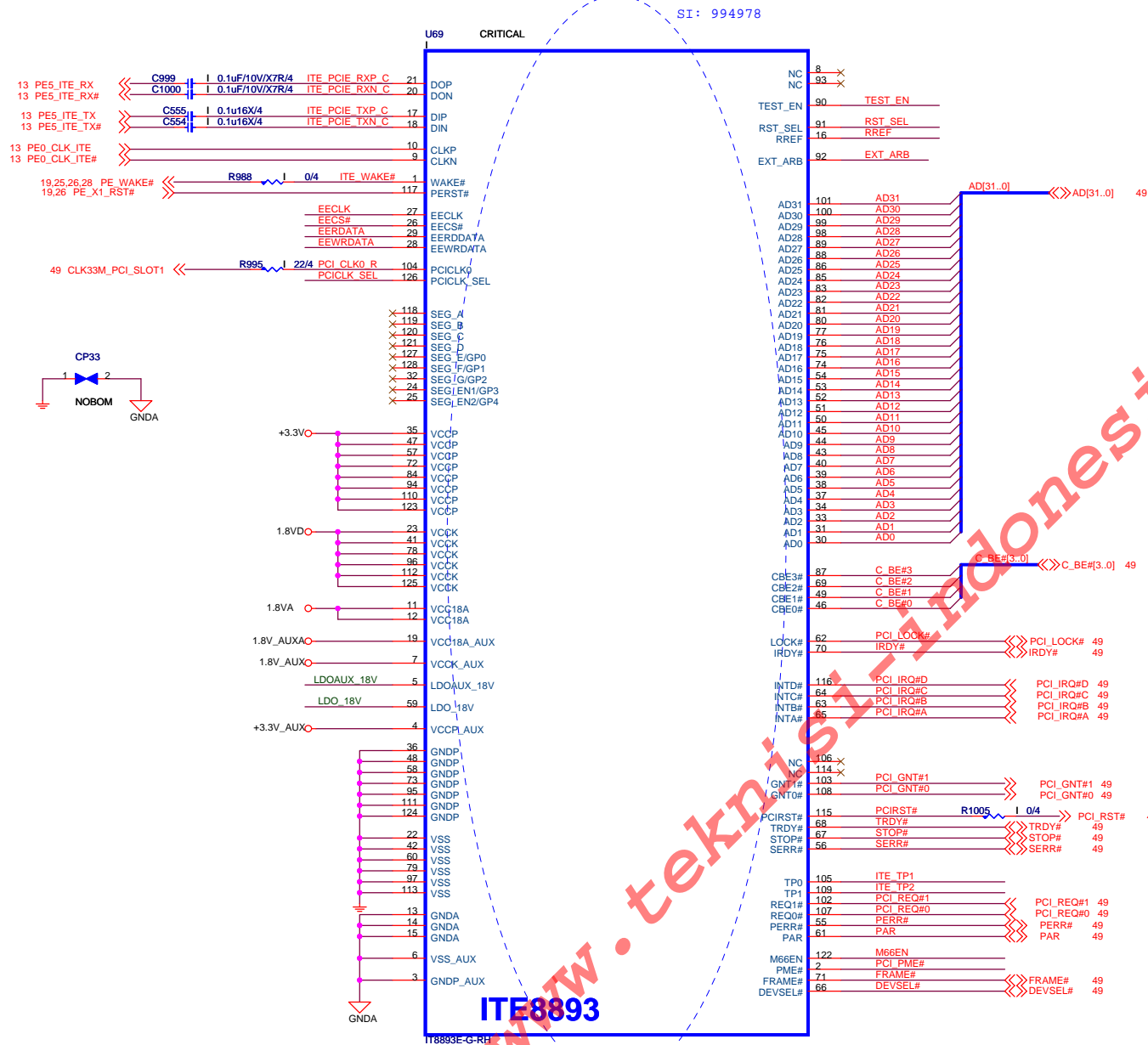
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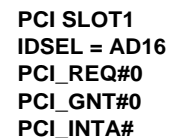
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Date:	Sheet 47 of 59	



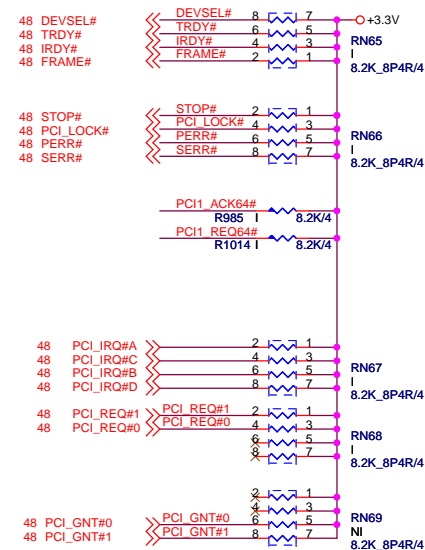
Release Date : Friday, April 25, 2014

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HP SCH P/N: 747866-000(MSI MS-7932)	
Size Custom	Document Description PCIe to PCI Bridge
Date:	Rev A
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PCI PULL-UP / DOWN RESISTORS



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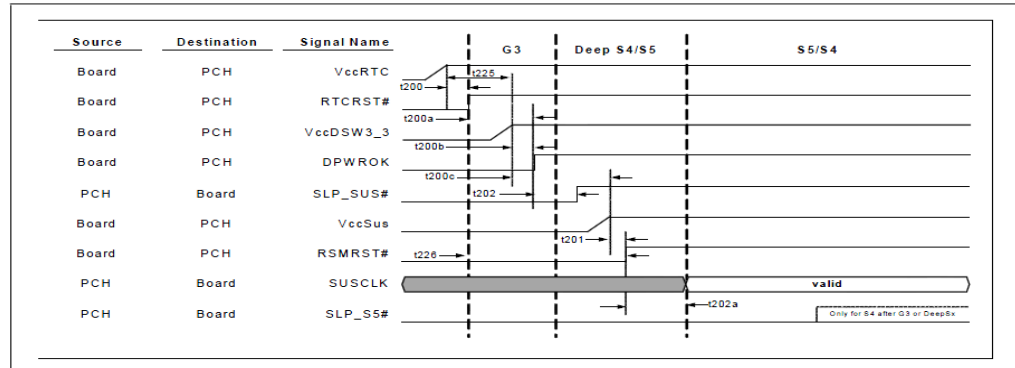


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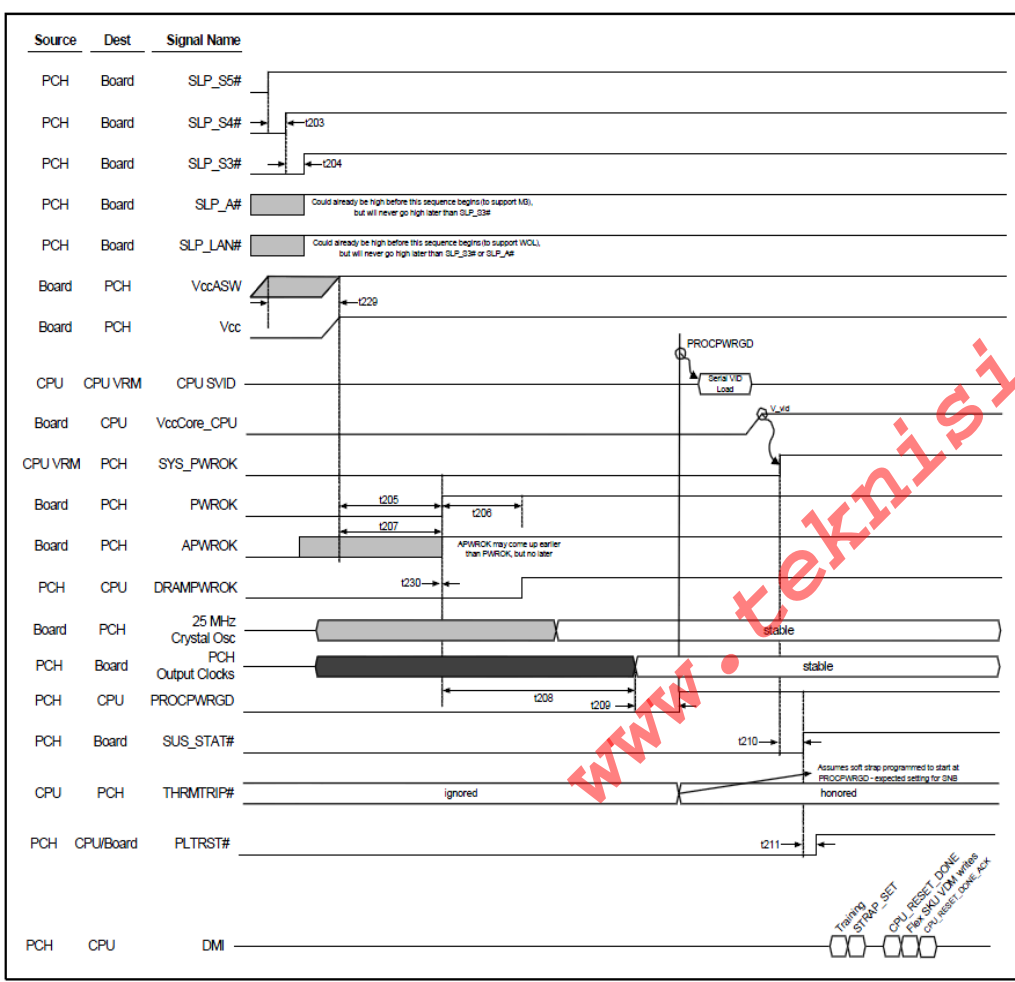
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Date:	Sheet	49	of	59
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G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



S5 to S0 Timing Diagram



G3-S5

ATX_5VSB

+3.3V_LPS

SLP_SUS#

LPS_ON#

+5V_AUX

+3.3V_AUX

RSMRST#

S5-S0

PWBTIN#

PWBTOUT#

SLP_S5/S4/S3

PSON#

+12V/+5V/+3.3V

VCC1_5/VCC_DDR

PCH_1P05

CHIP_PWROGD

MEM_PWROGD

H_PWROGD

VCCCP

PLTRST#

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HP SCH P/N: 747866-000(MSI MS-7932)

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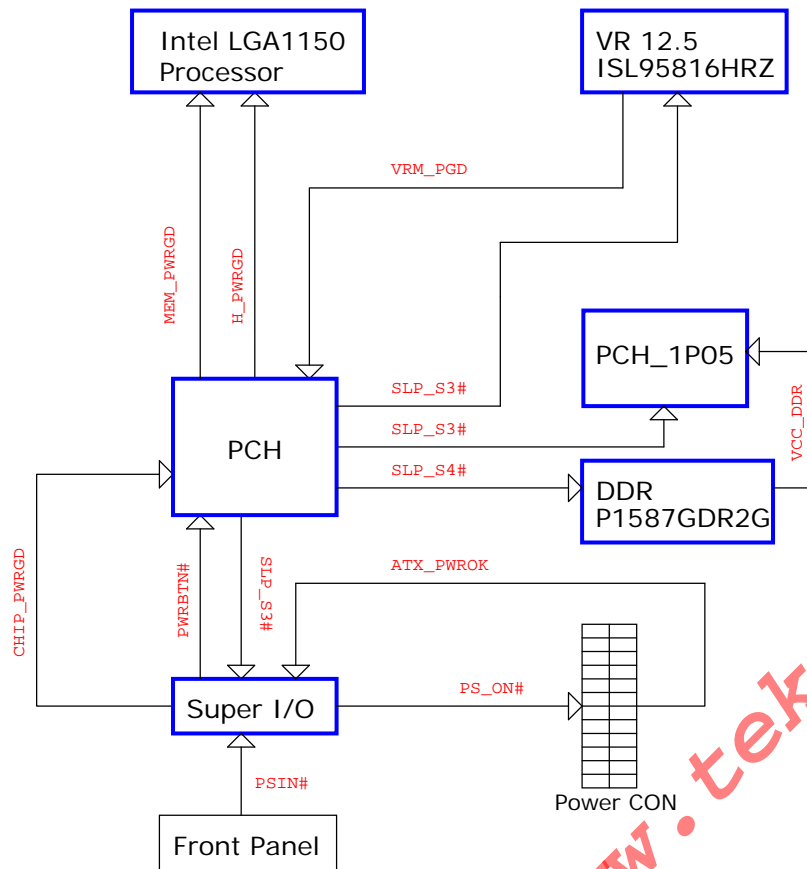
PON

Rev A

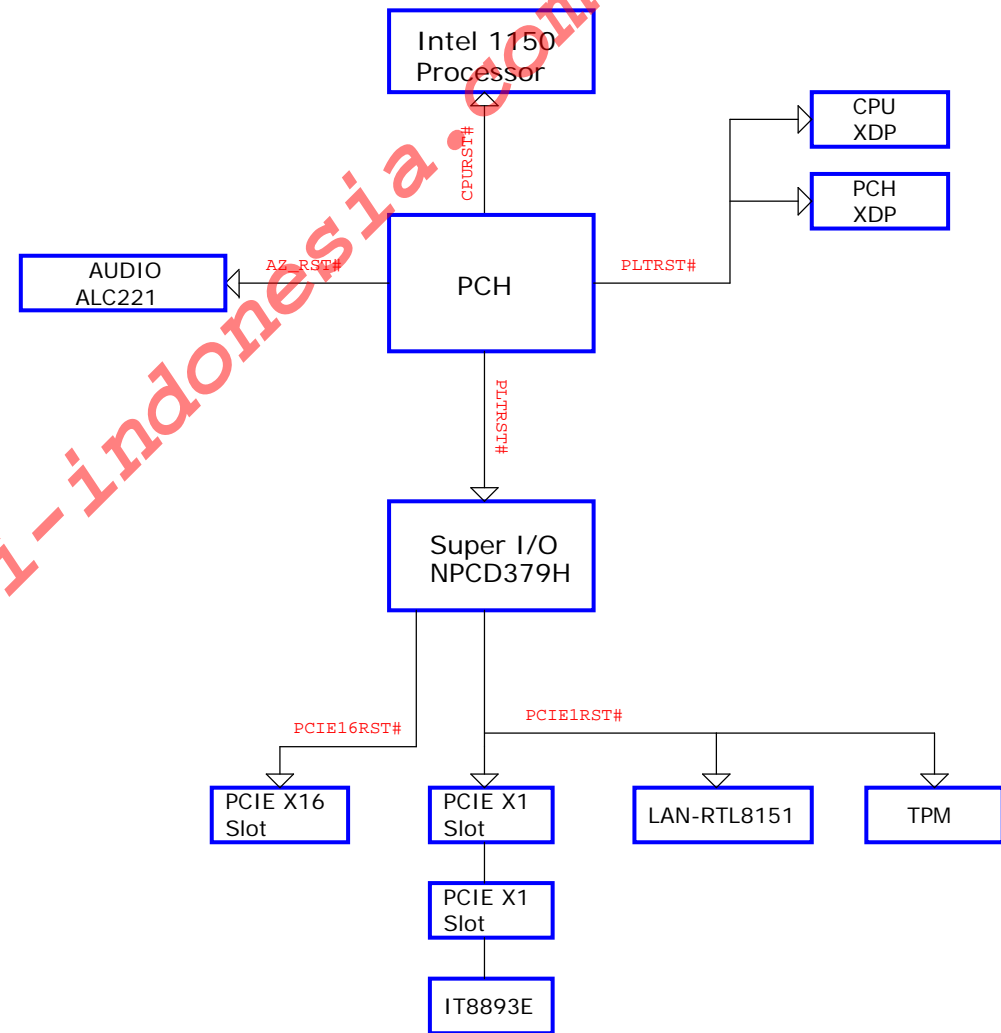
Date:

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PWROK MAP




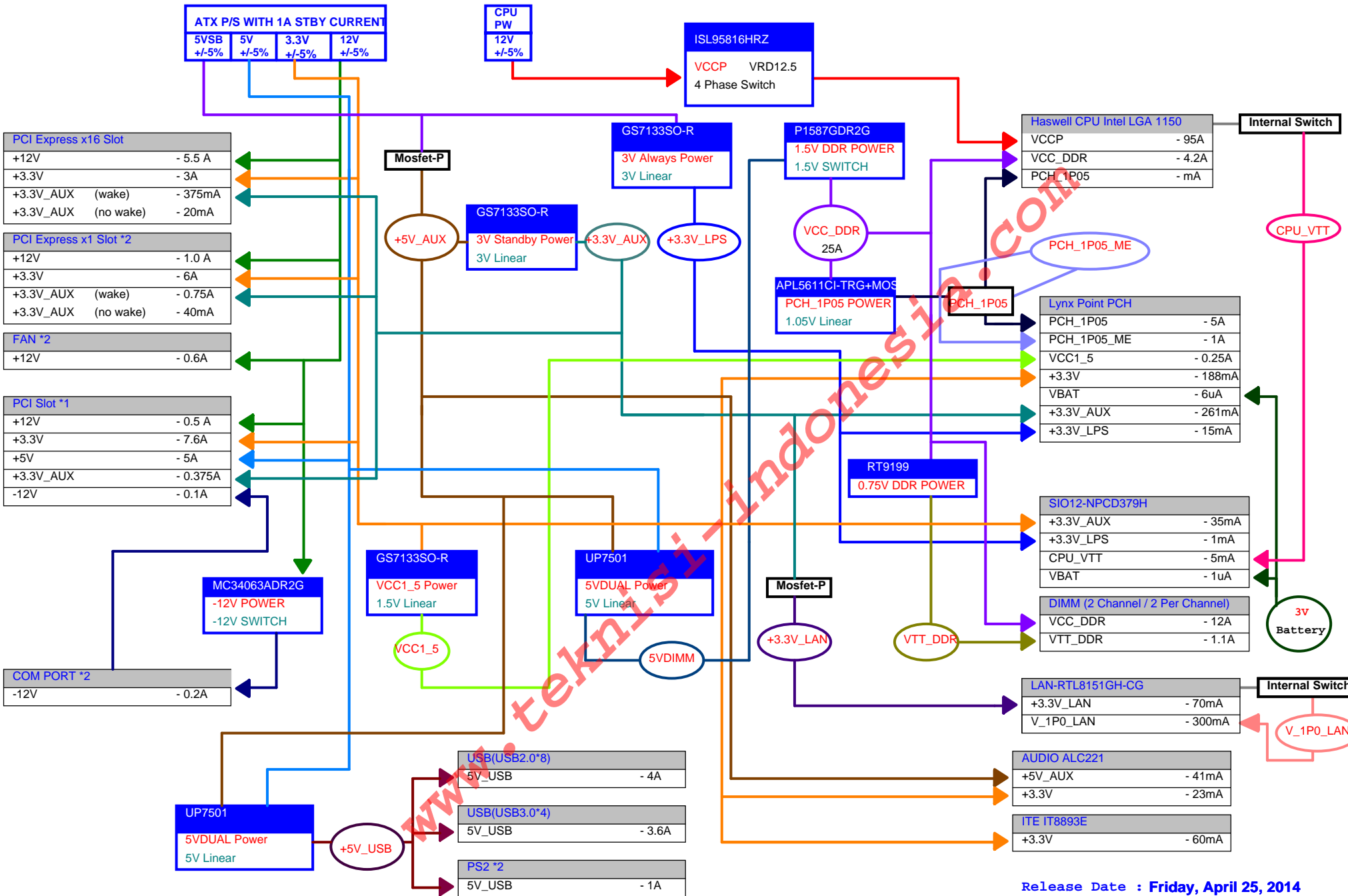
RESET MAP



Release Date : Friday, April 25, 2014

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			MICRO-STAR INT'L CO.,LTD	
			HP SCH P/N: 747866-000(MSI MS-7932)	
Size Custom	Document Description			Rev A
Pwrok/Reset				
Date:	Sheet 51 of 59			



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PCH

GPIO	I/O/NC	Power	Tol	Default	MB Function
GPIO[0]	I/O	Main	3.3V	GPI	FRONT_USB_P24_DET#
GPIO[1]	I/O	Main	3.3V	GPI	PCH_GPIO1
GPIO[2]	I/O	Main	5V	GPI	PCH_GPIO2
GPIO[3]	I/O	Main	5V	GPI	PCH_GPIO3
GPIO[4]	I/O	Main	5V	GPI	PCH_GPIO4
GPIO[5]	I/O	Main	5V	GPI	PCH_GPIO5
GPIO[6]	I/O	Main	3.3V	GPI	IO_SMI#
GPIO[7]	I/O	Main	3.3V	GPI	PCH_GPIO7
GPIO[8]	I/O	Resume	3.3V	GPO	PCH_GPIO8
GPIO[9]	I/O	Resume	3.3V	Native	USB_OCP#5
GPIO[10]	I/O	Resume	3.3V	Native	USB_OCP#6
GPIO[11]	I/O	Resume	3.3V	Native	PCH_SMBALERT#
GPIO[12]	I/O	Resume	3.3V	Native	LAN_DISABLE#
GPIO[13]	I/O	Resume	3.3V	GPI	INT_USB_P151_DET#
GPIO[14]	I/O	Resume	3.3V	Native	GPIO14
GPIO[15]	I/O	Resume	3.3V	GPO	PCH_GPIO15
GPIO[16]	I/O	Main	3.3V	GPI	PCH_GPIO16
GPIO[17]	I/O	Main	3.3V	GPI	PCH_GPIO17
GPIO[18]	I/O	Main	3.3V	Native	PCH_GPIO18
GPIO[19]	I/O	Main	3.3V	GPI	PCH_GPIO19
GPIO[20]	I/O	Main	3.3V	Native	PCIECLKREQ2#
GPIO[21]	I/O	Main	3.3V	GPI	FRONT_AUD_DET#
GPIO[22]	I/O	Main	3.3V	GPI	INT_USB_P150_DET#

GPIO[23]	I/O	Main	3.3V	Native	LDRQ1#
GPIO[24]	I/O	Resume	3.3V	GPO	PCH_GPIO24
GPIO[25]	I/O	Resume	3.3V	Native	BRD_ID2
GPIO[26]	I/O	Resume	3.3V	Native	PCH_GPIO26
GPIO[27]	I/O	DSW	3.3V	GPI	PCH_LAN_WAKE#
GPIO[28]	I/O	Resume	3.3V	GPO	PCH_GPIO28
GPIO[29]	I/O	Resume	3.3V	Native	SLP_WLAN#
GPIO[30]	I/O	Resume	3.3V	GPI	PCH_SUSWARN#
GPIO[31]	I/O	DSW	3.3V	GPI	PCH_GPIO31
GPIO[32]	I/O	Main	3.3V	GPO	PCH_GPIO32
GPIO[33]	I/O	Main	3.3V	GPO	PCH_GPIO33
GPIO[34]	I/O	Main	3.3V	GPI	PCH_GPIO34
GPIO[35]	I/O	Main	3.3V	GPO	BRD_REV0
GPIO[36]	I/O	Main	3.3V	GPI	PCH_GPIO36

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		MICRO-STAR INT'L CO.,LTD	
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Size Custom	Document Description GPIO Table1		Rev A
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PCH

GPIO	I/O/NC	Power	Tol	Default	MB Function
GPIO[37]	I/O	Main	3.3V	GPI	PCH_GPIO37
GPIO[38]	I/O	Main	3.3V	GPI	CHASSIS_ID0
GPIO[39]	I/O	Main	3.3V	GPI	BRD_ID1
GPIO[40]	I/O	Resume	3.3V	Native	USB_OCP#1
GPIO[41]	I/O	Resume	3.3V	Native	USB_OCP#2
GPIO[42]	I/O	Resume	3.3V	Native	USB_OCP#3
GPIO[43]	I/O	Resume	3.3V	Native	USB_OCP#4
GPIO[44]	I/O	Resume	3.3V	Native	PCIECLKREQ5#
GPIO[45]	I/O	Resume	3.3V	Native	PCH_GPIO45
GPIO[46]	I/O	Resume	3.3V	Native	PCH_GPIO46
GPIO[48]	I/O	Main	3.3V	GPI	CHASSIS_ID1
GPIO[49]	I/O	Main	3.3V	GPI	PCH_GPIO49
GPIO[50]	I/O	Main	3.3V	GPI	PCH_GPIO50
GPIO[51]	I/O	Main	3.3V	GPO	PCH_GPIO51
GPIO[52]	I/O	Main	3.3V	GPI	PCH_GPIO52
GPIO[53]	I/O	Main	3.3V	GPO	PCH_GPIO53
GPIO[54]	I/O	Main	3.3V	GPI	BOOT_BLK_EN#
GPIO[55]	I/O	Main	3.3V	GPO	PCH_GPIO55
GPIO[57]	I/O	Resume	3.3V	GPI	PCH_GPIO57
GPIO[58]	I/O	Resume	3.3V	Native	SML1CLK
GPIO[59]	I/O	Resume	3.3V	Native	USB_OCP#0
GPIO[60]	I/O	Resume	3.3V	Native	PCH_SML0ALERT#

GPIO[61]	I/O	Resume	3.3V	Native	PRNTER_DET#
GPIO[62]	I/O	Resume	3.3V	Native	SUS_CLK
GPIO[63]	I/O	Resume	3.3V	Native	SLP_S5#
GPIO[64]	I/O	CORE	3.3V	Native	CLKOUTFLEX0
GPIO[65]	I/O	CORE	3.3V	Native	CLKOUTFLEX1
GPIO[66]	I/O	CORE	3.3V	Native	CLKOUTFLEX2
GPIO[67]	I/O	CORE	3.3V	Native	CLKOUTFLEX3
GPIO[68]	I/O	CORE	3.3V	GPI	FRONT_USB_P26_DET#
GPIO[69]	I/O	CORE	3.3V	GPI	COMM_B_DET#
GPIO[70]	I/O	CORE	3.3V	GPI	BOOT_BLK_REC#
GPIO[71]	I/O	CORE	3.3V	GPI	BRD_ID0
GPIO[72]	I/O	DSW	3.3V	Native	PCH_GPIO72
GPIO[73]	I/O	Resume	3.3V	Native	BRD_REV1
GPIO[74]	I/O	Resume	3.3V	Native	PCH_SML1ALERT#
GPIO[75]	I/O	Resume	3.3V	Native	SML1DATA

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Size Custom	Document Description GPIO Table2		Rev A
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Pin	Default Function / Alternate Functions	Buffer Type	Buffer Power Wells	Motherboard Function
1	CLAMP_CTRL	OD _S	VS _{B3}	BLEED OFF CIRCUIT
2	SLP_S4#	IN _{TD4}	VS _{B3}	SLP_S4#
3	SLP_S5#	IN _{TD4}	VS _{B3}	SLP_S5#
4	SLP_S3#	IN _{TD4}	VS _{B3}	SLP_S3#
5	SIOPME#	OD _S O _{4B}	VS _{B3}	RI#
6	RSMRST#	O ₃₁₆	VS _{B3}	RSMRST#
7	PME_IN#	IN _{TD}	VS _{B3}	PME status
8	BLINK_OR	O ₂₀₂₀	VS _{B3}	Power LED driver
9	COLOR	O ₂₀₂₀	VS _{B3}	Power LED driver
10	VSS	I	GND	GND
11	PWRGD_OUT	OD _S	VS _{B3}	PWRGD_140ms
12	PS_ON#	OD _S	VS _{B3}	PS_ON#
13	TACH1	IN _{TD}	VDD3	SYS_FAN_TACH
14	CLOCKI32	IN _{TD}	VS _{B3}	SUS_CLK_IO
15	3V_AUX_SLOT_ON	O _{4B}	VS _{B3}	3V_AUX_SLOT_ON
16	VS _{B3}	I	PWR	VS _{B3}
17	VCORF	I	N/A	VCORF
18	LDRG#	O _{PC1}	VDD3	LDRG#
19	LAD3	IN _{PC} /O _{PC1}	VDD3	LAD3
20	LAD0	IN _{PC} /O _{PC1}	VDD3	LAD0
21	LAD2	IN _{PC} /O _{PC1}	VDD3	LAD2
22	VSS	I	PWR	GND
23	LAD1	IN _{PC} /O _{PC1}	VDD3	LAD1
24	SER_IRQ	IN _{PC} /O _{PC1}	VDD3	SERIRQ
25	PCI_RESET#	IN _{PC1}	VDD3	PLTRST#
26	PCI_CLK	IN _{PC1}	VDD3	33MHz
27	LFRANE#	IN _{PC1}	VDD3	LFRANE#
28	VS _{B3}	I	PWR	VS _{B3}
29	OPRST3#	O ₁₄	VS _{B3}	PCIE_X16 RESET#
30	INTRUDER#	IN _{TD}	V _{BAT}	HOOD_SENSE#
31	5V_USB_CTRL	O _{4B}	VS _{B3}	5V_USB_EN
32	HDLOCK#	OD ₁₂	VDD3	HOOD_LOCK#
33	GPIO01	IN _{TD} /OD ₉ O _{4B}	VS _{B3}	
34	HDUNLOCK#	OD ₁₂	VDD3	HOOD_UNLOCK#
35	HD_LED_IN#	IN _{TD}	VDD3	Hard Drive LED Input
36	CPU_PRNT1#	IN _{TSL}	V _{BAT}	CPU detection
37	VBAT	I	PWR	

38	12V_VSB_COMP	IN _{COMP2}	VS _{B3}	
39	COMP_IN3	IN _{COMP3}	VS _{B3}	
40	COMP_IN1	IN _{COMP1}	VS _{B3}	5V voltage monitor
41	COMP_IN2	IN _{COMP2}	VS _{B3}	12V voltage monitor
42	AVCC	I	PWR	AVCC
43	AD1	IN _{PC} /O _{PC1}	VDD3	AD1
44	AD2	IN _{PC} /O _{PC1}	VDD3	AD2
45	AD3	IN _{PC} /O _{PC1}	VDD3	AD3
46	FSPI_STR	IN _{TD}	AVCC	FSPI_STR
47	AGND	I	GND	AGND
48	PWBTOUT#	IN _{TD4}	VLPS	PWBTOUT#
49	PWBTIN#	IN _{TD4}	VLPS	PWBTIN#
50	LPS_WAKE	IN _{TD}	VLPS	LPS_WAKE
51	LPS_PHY#	O _{4B}	VLPS	LPS_PHY#
52	LPS_ON#	O _{4B}	VLPS	LPS_ON#
53	VLPS	I	PWR	VLPS
54	VTT	I	PWR	VTT
55	THERMTRIP#	IN _{AGTL}	VTT	THERMTRIP#
56	TSL_SCL	IN _{TD} /O _{TD1}	VTT	TSL_SCL
57	PROCHOT1#	IN _{AGTL} /OD _{AGTL24}	VTT	PROCHOT1#
58	PECI	IN _{PEC} /O _{PEC1}	VTT	PECI
59	PROCHOT2#	IN _{AGTL} /OD _{AGTL24}	VTT	PROCHOT2#
60	VSS	I	PWR	GND
61	PWM2	OD ₁₂ O _{6/12}	VDD3	SYS-FANPWM_REAR
62	HMSCL	IN _{2B} /OD _S	VS _{B3}	HMSCL
63	PWM1	OD ₁₂ O _{6/12}	VDD3	SYS-FANPWM_FRONT
64	HMSDA	IN _{2B} /OD _S	VS _{B3}	HMSDA
65	HD_LED_OUT	OD ₁₆	VS _{B3}	Hard Drive LED Output
66	WAKE_OUT#	OD ₁₂ O _{6/12}	VS _{B3}	Wake Disable Output
67	GPIO15(EV6#)	IN _{TD}	VS _{B3}	PCI_Express_Wake#
68	AMP_ON	O _{4B}	VS _{B3}	AMP_ON
69	AMP_ON#	O _{4B}	VS _{B3}	AMP_ON#
70	OPRST2#	O ₁₄	VS _{B3}	PE_RST#_OUT
71	12V_PG_25MS	OD _S	VS _{B3}	12V_PG_25MS
72	KBDRST#	IN _{TD} /OD ₁₄	VDD3	KBDRST#
73	AUDIO_BEEP	O _{4B}	VS _{B3}	DIAG Beep
74	TACH2	IN _{TD}	VDD3	TACH2
75	VS _{B3}	I	PWR	VS _{B3}
76	KBDAT	IN _{TD} /OD ₁₄	VDD3	KBDAT
77	MDAT	IN _{TD} /OD ₁₄	VDD3	MSDATA
78	SLIN_ASTRB#	OD ₁₄ O _{14/14}	VDD3	RSLIN#
79	KBCLK	IN _{TD} /OD ₁₄	VDD3	KBCLK
80	MCLK	IN _{TD} /OD ₁₄	VDD3	MCLK
81	PD3	IN _{TD} /O _{14/14}	VDD3	PD3
82	PD4	IN _{TD} /O _{14/14}	VDD3	PD4

83	INIT#	OD ₁₄ O _{14/14}	VDD3	INIT#
84	VSS	I	PWR	GND
85	PD1	IN _{TD} /O _{14/14}	VDD3	PD1
86	PD6	IN _{TD} /O _{14/14}	VDD3	PD6
87	PD0	IN _{TD} /O _{14/14}	VDD3	PD0
88	PD2	IN _{TD} /O _{14/14}	VDD3	PD2
89	PD7	IN _{TD} /O _{14/14}	VDD3	PD7
90	PD5	IN _{TD} /O _{14/14}	VDD3	PD5
91	STB_WWRITE#	OD ₁₄ O _{14/14}	VDD3	RSTB#
92	ERR#	IN _{TD}	VDD3	RERR#
93	VS _{B3}	I	PWR	VS _{B3}
94	AFD_DSTRB#	OD ₁₄ O _{14/14}	VDD3	RAFD#
95	PE	IN _{TD}	VDD3	RPE
96	GA20	IN _{TD} /O _{14/14}	VDD3	GA20
97	ACK#	IN _{TD}	VDD3	RACK#
98	SLCT	IN _{TD}	VDD3	RSCT
99	BUST_WAIT#	IN _{TD}	VDD3	RBUSY
100	TACH3	INTS	VDD3	TACH3
101	SMBTSDA	SW _{2B}	VDD3	SMB_DATA_MAIN
102	PWRGD_PS	IN _{TD4}	VS _{B3}	PWROK_PS
103	SMB2SDA	SW _{2B}	VDD3	SMB_DATA_RESUME
104	PWRGD_O2#	OD _S	VS _{B3}	PWRGD_50MS#
105	PWM3#	OD ₁₂ O _{6/12}	VDD3	PSU-FANPWM
106	5V_USB_MAIN#	OD _S	VS _{B3}	5V_USB_MAIN#
107	PWRGD_O1	OD _S	VS _{B3}	PWRGD_30MS
108	VSS	I	PWR	GND
109	SMB1SCL	SW _{2B}	VDD3	SMB_CLK_MAIN
110	SMB1#	OD _S	VDD3	IO_SMB1#
111	SMB2SDL	SW _{2B}	VDD3	SMB_CLK_RESUME
112	DSR1#	IN _{TD}	VDD3	DSRA#
113	RI1#	IN _{TD}	VDD3	RIA#
114	CTS1#	IN _{TD}	VDD3	CTSA#
115	DCD1#	IN _{TD}	VDD3	DCDA#
116	SIN1	IN _{TD}	VDD3	SINA
117	RTS1#	O _{4B}	VDD3	RTSA#
118	DTR#_BOUT1	O _{4B}	VDD3	DTRA#
119	SOUT1	O _{4B}	VDD3	SOUTA
120	DCD2#	IN _{TD}	VDD3	DCDB#
121	SOUT2	O _{4B}	VDD3	SOUTB
122	VS _{B3}	I	PWR	VS _{B3}
123	DTR#_BOUT2	O _{4B}	VDD3	DTRB#
124	RI2#	IN _{TD}	VDD3	RIB#
125	RTS2#	O _{4B}	VDD3	RTSB#
126	SIN2	IN _{TD}	VDD3	SINB
127	DSR2#	IN _{TD}	VDD3	DSRB#
128	CTS2#	IN _{TD}	VDD3	CTSB#

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(SI number: Gwen/Mordred)

2012/10/22

PAGE 7: Changed R436 from 3.16K ohm to 2.67K ohm.(SI number: 892595/892596)

PAGE 16: Modified R721 and R231 pull-up well from +5V_AUX to ATX_5VSB.(SI number: 892601/892602)

PAGE 20: Modified J68 to separated connector J66 and J67(HP spec change).(SI number: 892604/892605)

PAGE 22: Modified DP to DDI connector (HP spec change).

Add: J34.

Remove: C120,C117,C115,C110,C100,C108,C95,C98,C96,C99,C80,Q26,F2,R194,R199,
RN29,RN30,RN31,RN32,R421,R188,R210,R183,C132,R530,Q30,R196,
R278,Q28,R201,R206,U16,U45,U30,Q31,Q32,R211,R212,C149,C159,C165,C171,
C79,C71,R193,J64,L13,L12,L9,L11(SI number: 892607/892609)

PAGE 23: Modified DP header to DVID connector (HP spec change).

Remove: C121,C118,C111,C116,C101,C109,C97,C102,C103,C104,R202,R214,RN33,RN34,
RN35,RN36,L32,L33,L10,L34,R423,R215,R204,R185,C133,R544,Q51,R205,R279,
Q55,U17,U15,U39,Q40,R224,Q56,R222,C150,C162,C166,C174,C82,Q52,R217,R216,
F3,C83,C72,R223,P55

Add: C66,C69,C56,C57,C58,C61,C51,C53,R233,Q34,C81,U21,C76,C75,C84,U14,U6,
R181,R164,R173,R138,R140,R172,R103,R112,Q33,R170,R162,Q20,Q29,R166,R232,
RN21,RN22,RN23,RN24,L7,L8,L6,L5,R242,R276,R297,R299,D75,F1,FB4,C77,C1,
C2,R238,C168,J65(SI number:892611/892614)

PAGE 24: Modified J69 to J65(HP spec change).(SI number: 892615/892617)

PAGE30:Change audio mapping to follow reference circuit. C450
change to connect from ul3 pin17 to pin15: C451 change to
connect from ul3 pin16 to pin14 (SI number: 892619/892622)

PAGE30:Modify audio circuit by audio vendor review. FB12
connect to +3.3V,U19 pin9 connect to R918 and R844 (SI
number: 892625/892626)

PAGE31:Modify audio circuit by audio vendor review.
R413,U20,R396,C471,R415 changed to NI; added FB6,D78;
deleted D24 (SI number: 892625/892626)

PAGE32:Add USB switch control circuit
Added R530,Q92 (SI number: 892628/892629)

PAGE33:Deleted USB charging circuit by HP changed specification .
Deleted C181,C188,Q60,Q59,C186,C196,R725,R740,R112,R103,R299,R87,
C51,U38,R77,R232,R110,R118,U63,R893,R895,R892,R895,R892,C586,
R730,R138,R233,Q103,Q104 (SI number: 892633/892634)

PAGE34:Deleted USB P151 Header circuit by HP changed specification .
Deleted RN63,L4,RN46,L3,D3,C21,P151,C630 (SI number: 892635/892637)

PAGE35:Deleted USB2.0x2 connector and added USB3.0x2+USB2.0x2
connector circuit by HP changed specification . Deleted
J891,J82,JV81,RN60,L26,
RN61,L25,RN40,L19,RN41,L47,RN42,L50,RN43,
L48,C677,C278,C271,C266,C263,U27,U28,D30,C345; added
J10,JV10,D3,C21,RN63,L4,RN46,L3 (SI number: 892639/892640)

PAGE36:Added USB P152 Header circuit by HP changed specification . Added
U27,U28,D30,C345,C278,C271,RN42,L50,RN40,L19,RN60,L26,C726,P152(SI number: 892643/892645)

PAGE38:Modify Fan circuit ;EC6 and C204 changed from NI to I (SI number: 892646/892649)

PAGE39:Added EC cap for DDR power by power team suggestion ;Added EC27(SI number: 892651/892654)

PAGE40:Modify CPU power circuit by power team suggestion ;R104,R67,R96,R49 changed
from 6.2K to 6.34K ohm (SI number: 892656/892658)

PAGE44:Modify APS header circuit ;E18 pin 4 changed from SLP_S5# to +3.3V_AUX.
(SI number: 892659/892663)

2012/10/23

PAGE16:Reserve C540 for EMI.(SI number: 892666/892667)

PAGE20:Change FB13, FB14, FB15,FB16 from 0 ohm to 33 ohm for EMI.(SI number:892666/892667)

PAGE20:Add D61 for EMI.(SI number: 892666/892667)

PAGE24: Delete D10, D11 for EMI.(SI number: 892666/892667)

2012/10/24

PAGE 14: Modify R807 and R371 from 10k ohm to 499 ohm by Intel review.(SI number:893429)

PAGE 16: Rename PCIECLKREQ#5 to PCH_GPIO44 by Intel review.(SI number:893434)

PAGE 16: Rename PCIECLKREQ#2 to PCH_GPIO20 and modify R367 to NI by Intel review.(SI number:893434)

PAGE 24: Modify R285 and R292 from I to NI by Intel review.(SI number:893437)

PAGE 28: Add R920, R921,modify R900 to 0ohm, modify Q135 to 2N7002 by Intel review.(SI number:893435)

PAGE 21: Modify C445,C446 and C449 from NI to I by SIO vendor review.(SI number:893439)

PAGE 30: Modify C455 from 0.1uF to 10uF by audio vendor review.(SI number:892625)

2012/10/25

PAGE 42: Power team suggest to modify C647,C649,C644,C646,C648,C650,C652,
C653,C654,C655 from I to NI.(SI number:893441)

PAGE 17: Delete C683,C524 and add C960,C961,C962 by Intel review.(SI number:893898)

PAGE 43: Add C963,C964 by Intel review.(SI number:893898)

PAGE 16: Modify R738 from 2.2k ohm to 10k ohm,
modify R120 from 100k ohm to 10k ohm and modify to NI by Intel review.(SI number:893898)

2012/10/26

PAGE 44: Modify R747 from 75 ohm to 180 ohm and connect to +5V_AUX.(SI number:893677)

2012/10/30

PAGE 38: Delete 3/4 pin system fan colay circuit:
Delete: R36,C23,R499,R497,U67,R283,Q80,R236(SI number:896536)

PAGE 13: Modified PCIE clock mapping by HP requirement:
Connect PE6_CLK to J31, PE5_CLK to J32, PE0_CLK to J33.(SI number:894512)

PAGE 43: Modify EC1 from 270uF to 100uF by power team suggestion.(SI number:895385)

2012/11/01

PAGE 05: Modify DVI port mapping port D by HP requirement.(SI number: 894794)

2012/11/02

PAGE 45: Add C965, C966 for EMI.(SI number:896534)

2012/11/09

PAGE 23/24: Separate J65 (DVI+VGA) into J65 (DVI) and J69 (VGA).(SI number:892615/892617)

PAGE 14: Modified net PCH_GPIO1 to DC_DET# and connected to J34.(SI number:896525)

PAGE 40: Modified CPU PWM solution from NCP81102MNTXG to ISL95816HRZ.
Delete: R34,R1,C19,R31,R14,R15,C5,C18,R5,R13,R3,R16,C7,R4,R24,R30,C16,R22,R11,C17,R840,R7,R6,C15,R56,R55,R99,
R100,R131,RT3,R114,C40,R130,R91,R92,R74,R44,C26,R9,R32,C3,R63,R69,R62,C31,R90,R113,R122,R133,C46,
R81,R105,R104,C43,C44,R59,R70,R67,C34,C32,R82,R94,R98,C42,C38,R53,C24,C25,R49,R20,R28,R27,R39,RT1,
C12,C11,R19,R21,R10,C6,R124,R68,R108,R41,R107,R58,R89,R33,C20,R42,R35,R558.
Add: R70,R82,C23,R107,R58,R27,R45,R36,R105,C25,R87,C24,C34,C17,R110,R89,C42,C38,R53,R63,R55,R77,R92,C40,
R99,C46,R104,R30,C43,C12,R4,C4,R1,R24,R9,R14,R29,R91,C26,R2,C3,R6,C7,R3,R49,R15,R22,R16,R31R20,R8,
R44,R43,R42,R39,R19,R25,R28,C10,R100,R111,R108,C18,R52,R62,R90,R68,R94,R81,R61,C29,R59,R67,R69,R66,
R32,R74,R98,RT1,R21,C9,R23,C8,C6,R5,C11,R18,C13,R13,RT3.(SI number:896517)

2012/11/13

PAGE 31: Add R452, R453 and C524 and connect to pin 2 of P23 by HP suggestion.(SI number:)

PAGE 45: Add C183,C229,C245,C211,C171,C233,C253,C216,C185,C261,C264,C260,C172,C266,C530,C528,C676,C677,C534
by HP suggestion.(SI number:)

PAGE 47: Add C526 by HP suggestion.(SI number:)

PAGE 47: MH7 connect to GND by HP suggestion.(SI number:)

2012/11/14


PAGE 42: Modified EC24 from I to NI by power team suggestion.(SI number:898665)

PAGE 39: Add C173 by power team suggestion.(SI number:898666)

PAGE 45: Add C535, C536, C542,C543,C544 for EMI.(SI number:898667)

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Gwen X1

2012/11/20

PAGE 35: Separate J10 to J81 and J82 by HP spec change.(SI number:898670)
PAGE 40: Modified C24 to 4.7k ohm and modified NI to I by power team suggestion(SI number: 898673)
PAGE 22: Modify DP header to 2X10 pin by HP spec change.(SI number:898672)

Gwen/Mordred X2

2013/01/03

PAGE 29/35: The one PCB leverage proposal from MSI had been approved and will implement into EVT-2 phase. Modify J9 from RJ45+USB2.0 to RJ45+USB3.0 connector.(SI:913289)

PAGE 34: The one PCB leverage proposal from MSI had been approved and will implement into EVT-2 phase.Combine J81 and J82 USB 2.0 port to J10 USB2.0 X4 connector.(SI:913289)

PAGE 30:Rear Line in port malfunction. Modify R386 from 20k ohm to 39.2k ohm.(SI:903668,903669)

PAGE 44: UUT can not enter S5 Max Power Saving mode. Add R929 .(SI:906029,906030)

PAGE 43: There is no function for COM port.Connect Pin 8 of U35 to U5_SWC.(SI:902802)

PAGE 39: DDR power dynamic Load test is fail.
Moidy C496 from 1000pf to 470pf; Modify R247 from 2k ohm to 2.74k ohm;Modify R274 from 12k ohm to 7.68k ohm;Modify C324 from NI to I.(SI:910564,910565)

PAGE 17:amelot PCA Mordred/Gwen Schematic review bt Intel schematic review feedback .Add R932 .(SI:893898)

PAGE 31: Change front IO P23 pin2 from AGND to GND, Modify R453 to NI and R452 to I.(SI:913268)

2013/01/08

PAGE 16: A item of power on sequence signal integrity test is fail.Modify C129 from 2.2uf to luf.(SI:908764,908768)

PAGE 40: Modify HP Gwen/Mordred Cpu Power circuit to meet the test of Intel CPU power transient.
For Gwen:
Modify R32 from 4.7M ohm to 5.6M ohm.Modify R91 from 137K ohm to 110K ohm.Modify R92 from 3.83K ohm to 3.57K ohm.Modify C6 from 0.22uF to 0.47uF.
Modify C17 from 100pF to 68pF.Modify C26 from 0.01uF to 820pF(SI:905259)
Add Mordred colay parts:
PR32, PR91, PR92, PR29, PR110, PC6, PC11, PC17, PC26(SI:905260)

2013/01/14

PAGE 28: Use WAKE # signal can support OBFF function.
Modify R919 from I to N;Add Q151, Q152, Q153, R933, R934, R935, R936, R937, R951.(SI:912719)

PAGE 28: Modify Lan disable circuit to ensure same circuit with HP other projects.
Delete R900, R920, Q135 (SI:912753)

PAGE 32:+5 V_USB inrush current will cause the voltage drop.Delete Q92;
Add Q154, Q155,R938, R939, R940, C969, C970.(SI:911783,911786)

PAGE 43: +3.3V_AUX inrush current will cause the voltage drop of +5V_AUX.Modify R519 from 4.7k ohm to 20k ohm.
Add C968 and modify EC47 to NI.(SI:911788,911790)

PAGE 22: Modify DP connector circuit.
Modify P185 to PCIE X1 slot.
Delete FS2,R930,R931,R193,R174,R196,R183,R752.(SI:913444)

PAGE 16: Support SPI BIOS Quad IO Operation mode in EVT2 PCB.Modify R218, R220 to I.(SI:913300)

PAGE 24: Rise time ,fall time and pk-pk noise of D-Sub signal Integrity Items are fail.Modify L35,L36,L37,L38,L41,L51 to 33 nH.(SI:908746,908748)

2013/01/15

PAGE 36: 3 ports USB2.0 signal integrity test is fail.Modify D42,D30,L14,L15,L26 to I and modify RN55,RN56,RN60 to NI.(SI:910566,910567)

PAGE 30: Reserve this circuit to avoid ALC221 POP noise form CODE.
Delete R480,R198,R860,Q128,Q146.
Add Q160,Q161,R953,R954,R955,R956C982,D80.
Modify R953 from 1Kohm to 4.7Kohm. (SI:912682,912689)

PAGE 45: Add several stitching capacitors (layer change) in EVT2 PCB by MSI EMI engineers suggestion.
Add C983, C984 and C985. (SI:913414)

PAGE 43: Modify -12V circuit by MSI power engineer suggestion.
Add C986.
Modify EC1 to 270uF and R483 to 16.5k ohm. (SI:913414)

2013/01/28

PAGE 28: Modify +3.3V_LAN circuit to follow power design rule.
Modify R502 from 1K ohm to 30 ohm. (SI:916576)

Gwen/Mordred X3

2013/03/19

PAGE 40: Modify HP Gwen/Mordred Cpu Power circuit to meet the test of Intel CPU power transient.
Modify R3 from I to NI.
For Gwen:
Modify R91 from 110K ohm to 115K ohm.Modify C17 from 68 pF to 39 pF. (SI:905259)
For Mordred:
Modify PR91 from 113K ohm to 124K ohm. (SI:905260)

PAGE 38: Reserve TPM circuit.
Add U40,R959,R981,R957,R958,C850,C987,C988,C989,C990. (SI:929486)

PAGE 45: Reserve Dummy load circuit.
Add Q162,Q164,Q165,R960,R961,R962,R963,R964,R965,966,R967,R968,R969,R970,R971, R972,R973,R974,R975. (SI:908728)

PAGE 44: Modify +5V_AUX circuit to follow power design rule.
Add R984. (SI:916576)

PAGE 30: Reserve audio codec ALC221-VA and ALC221-VB colay circuit.
Add R976,R977,R978,R979,C991,C992. (SI:930271)

PAGE 28: Remove OBFF circuit.
Modify R919 from IN to I and delete Q151,Q152,R933,R934,R935,R951. (SI:912719)

PAGE 32: Use SLP_S4# to control USB switch IC.
Add R982 and R983. (SI:908728)

PAGE 43: Modify LDO Power circuit VCC1_5, +3.3V_AUX and +3.3V_LPS to meet the phase margin and gain margin test.
Modify C330 and C337 from NI to I. Modify C334 from 0.1uF to 0.033 uF for VCC1_5.
Modify EC47 from EL cap 1000uF to solid cap 100uF for +3.3V_AUX.
Modify R648 from 32.4K ohm to 324K ohm. Modify R638 from 10K ohm to 100K ohm for +3.3V_LPS. (SI:930329)

PAGE 45: Add several capacitors at +5V_USB by MSI EMI engineers suggestion.
Add C993 and C994 (SI:930302)


PAGE 21/30: Modify Amplifier Enable circuit to avoid ALC221 POP noise form CODE.
Add D81. Modify R953 from 4.7K ohm to 20K ohm. (SI:912682,912689)

PAGE 14: UUT shutdown after 8 error beep sounds if BBR jumper installed.
Add C995. Modify R226 from 1K ohm to 390 ohm. (SI: 924414,924417)

PAGE 14: Modify Board Rev to 01.
Modify R656 from NI to I and modify R653 from I to NI. (SI: 933025)

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Gwen/Mordred X3

2013/03/26

PAGE 46: Follow PCA spec and rename screw hole.
Rename MH1,MH2,MH3,MH4,MH5,MH6,MH7,MH8 to MTG1,MTG2,MTG3,MTG4,MTG5,MTG6,MTG7,MTG8. (SI: 932283)

PAGE 39/41/42: Follow PCA spec and modify cap size at PWM regulator high-side MOSFET drain .
Modify C31,C60,C86,C163,C196 size from 0805 to 1206. (SI: 932283)

2013/03/27

PAGE 22: Modify DP slot circuit.
Connect +5V to Pin A5 of P185. (SI: 932980)

PAGE 16/28: Modify crystal CL value according to crystal vendor test result.
Modify C942 from 27pF to 22pF. Modify C514 and C515 from 18pF to 15pF. (SI: 932989)

2013/04/09

PAGE 21: Remove the unused thermal sensor by thermal engineer suggestion.
Modify RT5,R610,C446 from I to NI. (SI: 935536)

PAGE 4: Modify thermtrip circuit according to Intel design guide.
Modify R213 from I to NI.(SI: 924414,924417)

Gwen/Mordred X4

2013/05/21

PAGE 30: Internal speaker has pop noise when UUT remove power cord.
Modify R200 to NI, Modify R733 from 20K ohm to 1K ohm,
Modify R734 from 20K ohm to 10K ohm and connect to +3.3V_AUX.
Add C996 and connect pin X of D80 to GND(SI: 943581)

PAGE 33/36: Follow PCA spec X81 pin definition to add USB2.0 port7 on P152.
Add RN64, L52 and U67. (SI: 935708)

PAGE 37: Motherboard have no PSWD jumper that makes BIOS password always be reset.
Modify JP49 from MP to I. (SI: 941138)

PAGE 43: Modify -12V circuit by msi power team engineer suggestion.
Modify C49 from 2200 pF to 1500 pF. (SI: 947863)

PAGE 1: Remove "ODM confidential" from schematic. (SI: 948604)

2013/05/27

PAGE 39: Modify DDR power circuit by msi power team engineer suggestion.
Modify R274 from 7.68K ohm to 9.53K ohm, modify R247 from 2.74K ohm to 3.74K ohm. (SI: 948994)

PAGE 40/42: Modify HP Gwen/Mordred CPU Power circuit to 3 phase support 84W.
Modify C42 and R89 from NI to I, modify R110 from 82K ohm to 100k ohm, modify R92 from 3.57K ohm to 3.6K ohm,
modify C26 from 820pf to 680pf, modify R91 from 115K ohm to 118K ohm, modify R21 from 487 ohm to 620 ohm,
modify R32 from 5.6M ohm to 6.2M ohm, Modify C6 from 0.47uF to 0.1uF, modify C11 from 0.33uF to 0.47uF,
modify C29,R94,R81,R59,R67,R69,R66,PR32,PR29,PR91,PR92,PR110,PC6,PC11,PC17,PC26,R188,C96,R194,C95,R187,C98,
U12,R244,R197,R266,Q11,Q21,Q12,R195,C109,CHOKE4,C680 to NI. (SI: 947654)

2013/05/29

PAGE 31: UUT has noise when play media file and plug in/pull out the MIC from front panel.
Reserve C997 and C998. (SI: 946837)

2013/06/10

PAGE 31: Remove retasking function.
Modify EC18 and EC23 from I to NI. Modify C997 and C998 from NI to I. (SI:946837)

PAGE 43: A item of power on sequence signal integrity test is fail.Modify R372
from 200K ohm to 1M ohm. Modify R538 from 10K ohm to 100K ohm.
Modify R536 from 29.4K ohm to 287K ohm(SI:949150)

2013/06/14

PAGE 44: The LED brightness and color looks not good on both Power LED and HDD LED.
modify R747 from 180 to 560 ohm. (SI: 936453)

PAGE 28: Disable GPIO12 function to support after G3 wake on lan.
Modify R900 from I to NI. (SI: 952714)

2013/06/14

PAGE 34/35/36/43/45: USB 2.0 R/W EMC test issue.
Modify C171,C172,C185,C216,C233,C245,C260,C261,C264,C411,C416,C423,C666,C667,C676,C677,C965 from 0.1uf and NI to 0.01uf and I.
Modify RN38,RN39,RN40,RN42,RN44,RN45,RN46,RN47,RN48,RN49,RN50,RN51,RN52,RN53,RN54,RN57,RN58,RN59,RN62,RN63 from I to NI.
Modify L43,L45,L22,L21,L42,L44,L46,L49 from NI to I.
Modify L3,L4,L28,L23,L27,L24,L16,L17,L18,L20,L50,L19 from NI to I,NI(SI: 950882)

Gwen/Mordred X5

2013/07/12

PAGE 20/45: Fix COM port ESD issue.
Modify C966 from NI to I and C766 from 100pf to varistor.(SI: 966671)

PAGE 14: Modify MB rev ID to 10
Modify R656, R632 from I to NI and modify R653, R629 from NI to I.

PAGE 30: Reserve audio codec ALC221-VA and ALC221-VB colay circuit.
Add C971,C972,C973,FB17,FB18,R987,R990,R991,R992,R993. (SI:964319)

PAGE 35/36: USB 2.0 R/W EMC test issue.
Modify L28,L23LL24,L27,L50,L19 from I,NI to NI. Modify RN62,R57,RN58,RN59,RN42,RN40 from NI to I,NI.
Modify RN51,RN52,RN53,RN54 from NI to I. Modify L14,L16,L18,L20 from NI to I (SI: 950882)

PAGE 43: Add a 30 ohm resistor on Q49 gate pin.
Add R1020. (SI:964320)

PAGE 32/33: USB3.0 HDD re-enumerate or lost intermittent.
Modify EC25,EC26,EC29,EC30,EC37 caps from 470uF to 1000uF. (SI:958227)

PAGE 21: Power LED blinks 4 times at low temperature during 11.2 strife test.
Modify R611 from 40K to 27.4K and modify R581 from 10K to 5.6K. (SI:955525)

PAGE 23: Fix DVI EMC test issue.
Modify RN21,RN22,RN23,RN24 from I to NI and modify L5,L6,L7,L8 from NI to I. (SI:964609)

PAGE 30/43: System power on - off continuity if 12V power did not connect.
Reserve D43, D82
Add Add Q166, R994, R1021 and R1022. Modify R538 from 100K to 10K, modify R536 from 287K to 29.4K,
modify R372 from 1M to 200K, modify R519 from 20K to 100K
R519 power well change to +3.3V_LPS from +5V_AUX.(SI: 961863)

Gwen/Mordred X5 to Gareth X1

2013/08/13

PAGE 9: Delete XMM4 slot circuit.
Delete XMM4,C257,C50.

PAGE 11: Delete XMM2 slot circuit.
Delete XMM2,C246,C55.

PAGE 22: Delete DDI port slot circuit.
Delete P185.

PAGE 26: Delete third PCIE X1 slot circuit.
Delete J33,C555,C554.

PAGE 33/36: Delete internal USB3.0 heard circuit.
Delete U67,U28,D30,RN60,L26,RN64,L52,RN40,L19,RN42,L50,C278,C271,C726,P152,C345.

PAGE 45: Delete +12V dummy load circuit.
Delete R973,Q165,Q162,R960,R961,R962,R963,R967,R968,R969,R970,R971,R972.

PAGE 48/49: Add ITE8893E PCIE to PCI circuit.
Add
C999,C1000,C554,C555,R988,R995,CP33,U68,C1033,R1003,R996,R997,R998,R1000,R999,R1001,R1002,R989,R1008,
R1009,R1015,R1016,R1019,C1023,C1022,C1021,C1036,C1035,C1034,C1039,C1038,C1037,C1040,C1041,C1042,C1014,
C1012,C1017,C1019,L52,L53,C1015,C1013,C1018,C1020,L54,L55,C1016,J20,R1012,EC69,EC70,C1025,C1027,C1029,
C1031,C1028,C1030,C1032,RN65,RN66,R985,R1014,RN67,RN68,RN69.

PAGE 34/36/45: Reserve some cap for EMI.
Add C1043,C1044,C1045,C1046,C1047,C1048,C1049.

PAGE 14: Modify board ID to 010 for Gareth.
Modify R713,R637 to NI and modify R716,R651 to I.(SI:990833)

2013/09/13

PAGE 49: Added PCI JTAG pullup/down resistors and decouple caps for PRSNT1#2#
Add R1023,R1024,R1025,R1026,C1050,C1051.(SI:987842)


2013/09/16

PAGE 19: Reserve a pull-up resistor at Pin 100 of SIO.
Add R1027. (SI:988479)

PAGE 1: update HP PN in schematic.(SI:988317/992020)

2013/10/11

PAGE 48: Confirm implement the latest ITE8893
PCI bridge version into PVT build.
Modify PCI bridge to IT8893E version G.
(SI: 994978)



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Gareth REV A:

PAGE 14: Change revision to "A" and modify REV ID to 00 .
Modify R629 from I to NI. Modify R632 from NI to I. (SI: 1009334)


PAGE 41: Modify CPU 2*2 power connector silkscreen.
Modify P3 to P2. (SI: 1009337)

PAGE 46: Remove soldermask of pins for debug ports
DBG4, JXDP1 and DBG1 footprint changed to another ones without soldermask on pins. (SI:1009313)

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